DOCKET NO. NL000095 (PHIL06-00095) PATENT

#13 Appeal Brief 10/16/03 K. Tannen

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Adolphe Johannes Gerardus Ruigt
Serial No.:	09/801,625
Filed:	March 8, 2001
For:	LIQUID CRYSTAL DISPLAY DEVICE
Group No.:	2673
Examiner:	Vincent E. Kovalick

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

APPEAL BRIEF

The Appellant has appealed to the Board of Patent Appeals and Interferences from the decision of the Examiner dated May 6, 2003, finally rejecting Claims 1, 2, 4-8, 10-15, and 17-19. The Appellant filed a Notice of Appeal on July 7, 2003, which was received by the U.S. Patent and Trademark Office on July 11, 2003. The Appellant respectfully submits this brief on appeal, in triplicate, with a statutory fee of $320.00.

REAL PARTY IN INTEREST

This application is currently owned by U.S. Philips Corporation as indicated by an assignment recorded on June 4, 2001 in the Assignment Records of the United States Patent and Trademark Office at Reel 011864, Frame 0969.

RELATED APPEALS AND INTERFERENCES

There are no known appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this pending appeal.

STATUS OF CLAIMS

Claims 1, 2, 4-8, 10-15, and 17-19 stand rejected pursuant to a final Office Action mailed May 6, 2003. Claims 3, 9, and 16 stand objected to as being allowable if rewritten in independent form to incorporate the elements of their respective base claims and any intervening claims. Claims 1, 2, 4-8, 10-15, and 17-19 are presented for appeal. Claims 1-19 are shown in Appendix A.

STATUS OF AMENDMENTS

The Appellant submitted an Amendment and Response to Final Office Action on July 7, 2003. The Amendment and Response amended Claim 1 to correct an informality noted by the Appellant. The Examiner refused to enter the amendment, asserting that it failed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal.

SUMMARY OF INVENTION

According to one embodiment, a liquid crystal display ("LCD") device includes a liquid crystal cell (element 1). (*Page 3, Lines 6-7*). The liquid crystal cell includes a liquid crystal material (element 2) between two supporting plates or substrates (elements 3 and 4). (*Page 3, Lines 7-8*). The liquid crystal cell also includes selection electrodes (element 5) and data electrodes (element 6). (*Page 3, Lines 9*). A power supply source (element 17) provides the operating voltage in the LCD device. (*Page 3, Lines 22-24*).

The LCD device further includes a measuring element (element 9) connected to a control section (element 13). (*Page 3, Lines 25-27*). A current through the measuring element and an effective voltage across the measuring element may be used to adjust the operating voltage of the LCD device. (*Page 2, Lines 5-8; Page 4, Lines 1-8*).

STATEMENT OF ISSUES

Are Claims 1, 2, 4-8, 10-15, and 17-19 obvious under 35 U.S.C. § 103(a)?

GROUPING OF CLAIMS

Pursuant to 37 C.F.R. § 1.192(c)(7), the Appellants request that Claims 1, 2, 4-8, 10-15, and 17-19 be grouped together for purposes of this appeal.

ARGUMENT

The rejection of Claims 1, 2, 4-8, 10-15, and 17-19 under 35 U.S.C. § 103(a) is improper and should be withdrawn.

A. OVERVIEW

Claims 1, 7, 13, 14, and 19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,500,538 to Yamazaki et al. ("*Yamazaki*") and U.S. Patent No. 5,589,960 to Chiba et al. ("*Chiba*") in view of U.S. Patent No. 6,310,598 to Koyama et al. ("*Koyama*"). Claims 2, 4, 8, 10, 15, and 17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yamazaki*, *Chiba*, and *Koyama* in further view of U.S. Patent No. 6,412,977 to Black et al. ("*Black*"). Claim 5 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yamazaki*, *Chiba*, and *Koyama* in further view of U.S. Patent No. 4,298,866 to Hodemaekers ("*Hodemaekers*"). Claims 6, 11, and 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yamazaki*, *Chiba*, and *Koyama* in further view of U.S. Patent No. 5,940,184 to Okabe ("*Okabe*"). Claim 12 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yamazaki*, *Chiba*, and *Koyama* in further view of U.S. Patent No. 6,466,204 to Oh ("*Oh*").

A copy of Claims 1-19 is provided in Appendix A. A copy of *Yamazaki* is provided in Appendix B. A copy of *Chiba* is provided in Appendix C. A copy of *Koyama* is provided in Appendix D. A copy of *Black* is provided in Appendix E. A copy of *Hodemaekers* is provided in Appendix F. A copy of *Okabe* is provided in Appendix G. A copy of *Oh* is provided in Appendix H.

B. STANDARD

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. (*MPEP § 2142; In re Fritch, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992)*). The initial burden of establishing a *prima facie* basis to deny patentability of a claimed invention is always upon the Patent Office. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984)*). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993)*). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. (*In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Grabiak, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985)*).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. (*In re Bell, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993)*). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references

when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. (*MPEP § 2142*).

C. THE *YAMAZAKI* REFERENCE

Yamazaki recites an electro-optical device that includes pixels arranged in rows and columns. (*Abstract*). Each pixel includes a pair of thin film transistors (TFTs), one p-channel TFT and one n-channel TFT. (*Abstract*).

D. THE *CHIBA* REFERENCE

Chiba recites a double-layer liquid crystal display system. (*Abstract*). The system includes a liquid crystal display device for displaying characters and/or graphical forms. (*Abstract*). The system also includes a compensating liquid crystal device that compensates for the optical phase of the liquid crystal display device. (*Abstract*). A photo sensor and a temperature sensor are used to adjust the "drive voltage" of the double-layer liquid crystal display system. (*Col. 4, Lines 8-19*). The photo sensor detects the contrast of a display on the liquid crystal display device as observed through the compensating liquid crystal device. (*Col. 4, Lines 16-19*). The temperature sensor measures the ambient temperature of the liquid crystal display device. (*Col. 4, Lines 8-10*).

E. THE *KOYAMA* REFERENCE

Koyama recites a display device that includes a pixel matrix, a signal line drive circuit, and a scanning line drive circuit. (*Abstract*). The pixel matrix includes thin film transistors (TFTs) or other switching elements arranged in a matrix, and individual TFTs are controlled using signals produced by the two line drive circuits. (*Col. 1, Lines 16-25*). The display device also includes one or more threshold value control circuits. (*Figures 1 and 12*). The threshold value control circuits control the signals produced by the line drive circuits. (*Abstract*).

F. CLAIMS 1, 2, 4-8, 10-15, AND 17-19

Claim 1 recites:

> A liquid crystal display device comprising a first substrate provided with one or more first electrodes and a second substrate provided with one or more second electrodes, and a twisted nematic liquid crystal material between the two substrates, in which, viewed perpendicularly to the substrates, overlapping parts of the electrodes define pixels, characterized in that the display device is provided with means for adjusting an operating voltage of the liquid crystal display device based on one or more measurements involving a measuring element positioned between the first and second substrates.

The proposed *Yamazaki–Chiba–Koyama* combination fails to disclose, teach, or suggest all elements of Claim 1.

The Examiner admits that *Yamazaki* fails to disclose "means for adjusting an operating voltage of the liquid crystal display device based on one or more measurements involving a measuring element positioned between the first and second substrates" as recited in Claim 1. (*05/06/03 Office Action, Page 3, First paragraph*). The Examiner asserts that *Chiba* recites the

use of a measuring element but admits that *Chiba* fails to disclose the use of a measuring element "positioned between the first and second substrates" as recited in Claim 1. (*05/06/03 Office Action, Page 3, First paragraph*).

The Examiner asserts that *Koyama* discloses the use of a measuring element positioned between two substrates and that it would be obvious to combine *Koyama* with the teachings of *Yamazaki* and *Chiba*. (*05/06/03 Office Action, Page 3, Last paragraph – Page 4, First paragraph*).

Koyama simply recites a display device that alters the signals provided to TFTs or other switching elements. *Koyama* lacks any mention of using a "measuring element" that is "positioned between" two substrates to alter the signals provided to the TFTs. In fact, *Koyama* lacks any mention of using a "measuring element."

The Examiner asserts that *Koyama* discloses the use of a "measuring element" that is "positioned between" two substrates at column 1, lines 64-67 and column 2, lines 1-4. (*05/06/03 Office Action, Page 3, Second paragraph*). However, this portion of *Koyama* simply states that a previous "active matrix type liquid-crystal display unit" uses thin film transistors made of polysilicon. (*Col. 1, Lines 64-66*). This portion of *Koyama* also states that in this previous unit, a signal line drive circuit and a scanning line drive circuit were formed on "a glass substrate" along with the pixel matrix. (*Col. 1, Line 67 – Col. 2, Line 3*).

This portion of *Koyama* contains no mention of a "measuring element" that is "positioned between" two substrates. In fact, this portion of *Koyama* lacks any mention of a "measuring element" at all. In addition, this portion of *Koyama* only refers to "a glass substrate" and fails to

recite the use of multiple substrates. As a result, this portion of *Koyama* fails to disclose, teach, or suggest a "measuring element" that is "positioned between" two substrates as recited in Claim 1.

The Examiner also asserts that by combining *Chiba* and *Koyama*, the sensors taught by *Koyama* would be placed on a substrate as taught by *Chiba*. (*05/06/03 Office Action, Page 3, Second paragraph*).

Chiba simply recites the use of a photo sensor and a temperature sensor. *Chiba* lacks any mention of placing these sensors on a substrate or between two substrates. In fact, as clearly shown in Figure 3 of *Chiba*, the photo and temperature sensors are separate from the liquid crystal display device (element 11) and the compensating liquid crystal device (element 13).

Moreover, the Examiner has not shown that the sensors of *Chiba* could operate properly if placed between two substrates of a liquid crystal device. The purpose of the photo sensor is to measure the contrast of an image produced by the display system of *Chiba*. Placing the photo sensor between substrates in a liquid crystal device would prevent the sensor from detecting the contrast of the final image produced by the display system of *Chiba*. As a result, this modification would render *Chiba* unsuitable for its intended purpose.

The purpose of the temperature sensor is to measure ambient temperature, or the temperature surrounding or encompassing the display system of *Chiba*. Placing the temperature sensor between the substrates in a liquid crystal device would prevent the sensor from detecting the temperature surrounding the display system of *Chiba*. As a result, this modification would also render *Chiba* unsuitable for its intended purpose. Because of this, one skilled in the art

would not be motivated to place the sensors of *Chiba* between two substrates as asserted by the Examiner.

For these reasons, the proposed *Yamazaki–Chiba–Koyama* combination fails to disclose, teach, or suggest the Appellant's invention recited in Claim 1. As a result, Claim 1 is patentable over the proposed *Yamazaki–Chiba–Koyama* combination. Claims 7 and 14 contain elements that are analogous to the novel and non-obvious elements recited in Claim 1. As a result, Claims 7 and 14 are patentable over the proposed *Yamazaki–Chiba–Koyama* combination. At a minimum, Claims 2, 4-6, 8, 10-13, 15, and 17-19 are patentable due to their dependence from allowable base claims.

CONCLUSION

The Appellant has demonstrated that the present invention as claimed is clearly distinguishable over the prior art cited of record. Therefore, the Appellant respectfully requests the Board of Patent Appeals and Interferences to reverse the final rejection of the Examiner and instruct the Examiner to issue a notice of allowance of all claims.

The Appellant has enclosed a check in the amount of $320.00 to cover the cost of this Appeal Brief. The Appellant does not believe that any additional fees are due. However, the Commissioner is hereby authorized to charge any additional fees or credit any overpayments to Davis Munck Deposit Account No. 50-0208. No extension of time is believed to be necessary. If an extension of time is needed, however, the extension is requested. Please charge the fee for the extension to Deposit Account No. 50-0208.

Respectfully submitted,

DAVIS MUNCK, P.C.

Date: Sept. 11, 2003

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APPENDIX A

PENDING CLAIMS

1. A liquid crystal display device comprising a first substrate provided with one or more first electrodes and a second substrate provided with one or more second electrodes, and a twisted nematic liquid crystal material between the two substrates, in which, viewed perpendicularly to the substrates, overlapping parts of the electrodes define pixels, characterized in that the display device is provided with means for adjusting an operating voltage of the liquid crystal display device based on one or more measurements involving a measuring element positioned between the first and second substrates.

2. A liquid crystal display device as claimed in claim 1, characterized in that the means for adjusting the operating voltage of the display device comprise means for measuring a current through the measuring element.

3. A liquid crystal display device as claimed in claim 2, characterized in that the means for adjusting the operating voltage of the display device comprise means for raising the operating voltage and simultaneously measuring the current through the measuring element.

4. A liquid crystal display device as claimed in claim 2, characterized in that the means for adjusting the operating voltage of the display device comprise means for raising the operating voltage and measuring a peak current through the measuring element.

5. A liquid crystal display device as claimed in claim 1, characterized in that the means for adjusting the operating voltage of the display device comprise means for measuring a capacitance of the measuring element.

6. A liquid crystal display device as claimed in claim 1, characterized in that the measuring element comprises a portion of the liquid crystal material.

7. A liquid crystal display device, comprising:

a first substrate comprising one or more first electrodes;

a second substrate comprising one or more second electrodes;

a liquid crystal material between the first and second substrates, wherein at least portions of the electrodes that overlap when viewed define pixels;

a measuring element positioned between the first and second substrates; and

a controller operable to adjust an operating voltage of the liquid crystal display device based on one or more measurements involving the measuring element.

8. The liquid crystal display device of Claim 7, wherein the one or more measurements measure at least one of:

a current through the measuring element;

a peak current through the measuring element; and

a capacitance of the measuring element.

9. The liquid crystal display device of Claim 7, wherein the controller is operable to adjust the operating voltage of the liquid crystal display device such that a transmission strength of the pixels is fifty percent of a maximum transmission strength.

10. The liquid crystal display device of Claim 7, wherein the controller is operable to adjust the operating voltage of the liquid crystal display device at varying ambient temperatures.

11. The liquid crystal display device of Claim 7, wherein the measuring element comprises a portion of the liquid crystal material.

12. The liquid crystal display device of Claim 7, further comprising a power supply operable to provide the operating voltage.

13. The liquid crystal display device of Claim 7, wherein the liquid crystal material comprises twisted nematic liquid crystal material.

14. A method, comprising:

identifying at least one operational characteristic of a measuring element positioned between a first substrate and a second substrate of a liquid crystal display device; and

adjusting an operating voltage of the liquid crystal display device based on the at least one identified operational characteristic.

15. The method of Claim 14, wherein the at least one operational characteristic of the measuring element comprises at least one of:

a current through the measuring element;

a peak current through the measuring element; and

a capacitance of the measuring element.

16. The method of Claim 14, wherein adjusting the operating voltage of the liquid crystal display device comprises adjusting the operating voltage such that a transmission strength of pixels displayed the liquid crystal display device is fifty percent of a maximum transmission strength.

17. The method of Claim 14, wherein adjusting the operating voltage of the liquid crystal display device comprises adjusting the operating voltage at varying ambient temperatures.

18. The method of Claim 14, wherein the measuring element comprises a portion of a liquid crystal material between the first and second substrates.

19. The method of Claim 14, wherein the liquid crystal material comprises twisted nematic liquid crystal material.

APPENDIX B

***Yamazaki* Reference**

U.S. Patent No. 5,500,538

US005500538A

United States Patent [19]

Yamazaki et al.

[11] Patent Number: 5,500,538

[45] Date of Patent: Mar. 19, 1996

[54] **ELECTRO-OPTICAL DEVICE AND METHOD OF DRIVING THE SAME**

[75] Inventors: **Shunpei Yamazaki**, Tokyo; **Akira Mase**, Aichi, both of Japan

[73] Assignee: **Semiconductor Energy Laboratory Co., Ltd.**, Kanagawa, Japan

[21] Appl. No.: **314,714**

[22] Filed: **Sep. 29, 1994**

Related U.S. Application Data

[62] Division of Ser. No. 104,935, Aug. 12, 1993, Pat. No. 5,383,041, which is a continuation of Ser. No. 805,521, Dec. 13, 1991, abandoned.

[30] **Foreign Application Priority Data**

Dec. 20, 1990 [JP] Japan 2-418664
Dec. 29, 1990 [JP] Japan 2-418291

[51] **Int. Cl.**[6] **H01L 29/04**; H01L 31/036; H01L 21/0376

[52] **U.S. Cl.** **257/49**; 257/56; 257/59; 257/72; 257/102; 359/54; 359/59; 359/57; 359/85

[58] **Field of Search** 257/59, 72, 56, 257/102, 49; 359/59, 85, 57, 54

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,818,077	4/1989	Ohwada et al.	350/350.5
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5,383,041	1/1995	Yamazaki et al.	359/59

FOREIGN PATENT DOCUMENTS

53-144297	12/1978	Japan	359/59
6396636	4/1988	Japan	359/59
1068724	3/1989	Japan	340/784
1107237	4/1989	Japan	340/784

Primary Examiner—William Mintel
Attorney, Agent, or Firm—Sixbey, Friedman, Leedom & Ferguson; Gerald J. Ferguson, Jr.; Evan R. Smith

[57] **ABSTRACT**

An electro-optical device is disclosed. The electro-optical device comprises pixels arranged in rows and columns. Each pixel comprises at least one complementary TFT (thin film transistor) pair. Each complementary TFT pair consists of an n-channel TFT and a p-channel TFT. The gates of the complementary TFTs of each pixel are all connected to a signal line extending in the Y-direction. The input terminals of the TFTs of each pixel are connected to a pair of signal lines extending in the X-direction. Each pixel has at least one pixel electrode connected to the outputs of the TFTs thereof. In the operation of the electro-optical device, an electric signal is applied to the pair of signal lines extending in the X-direction and an electric signal is applied to the signal line extending in the Y-direction for the duration of the electric signal applied to the pair of signal lines extending in the X-direction.

23 Claims, 23 Drawing Sheets

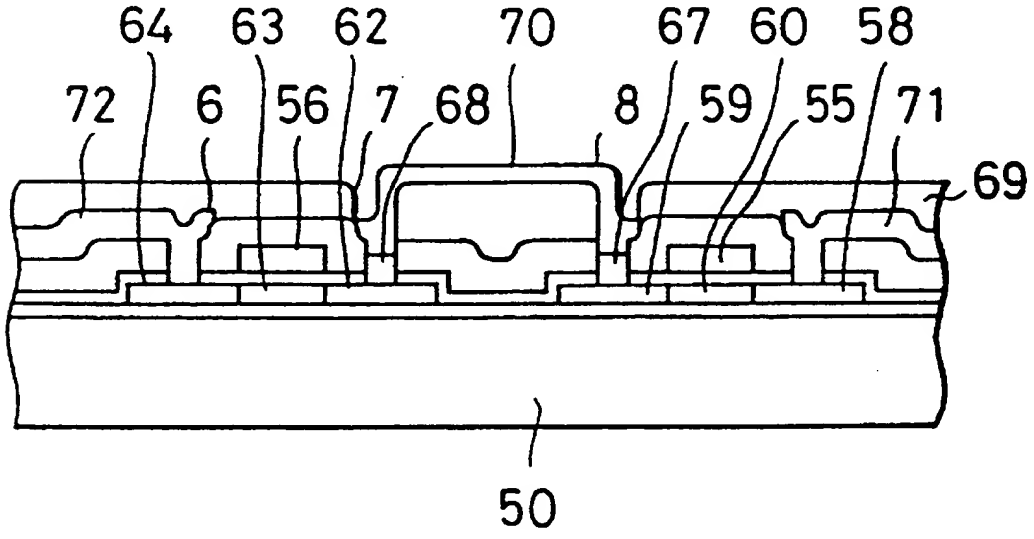


FIG. 1

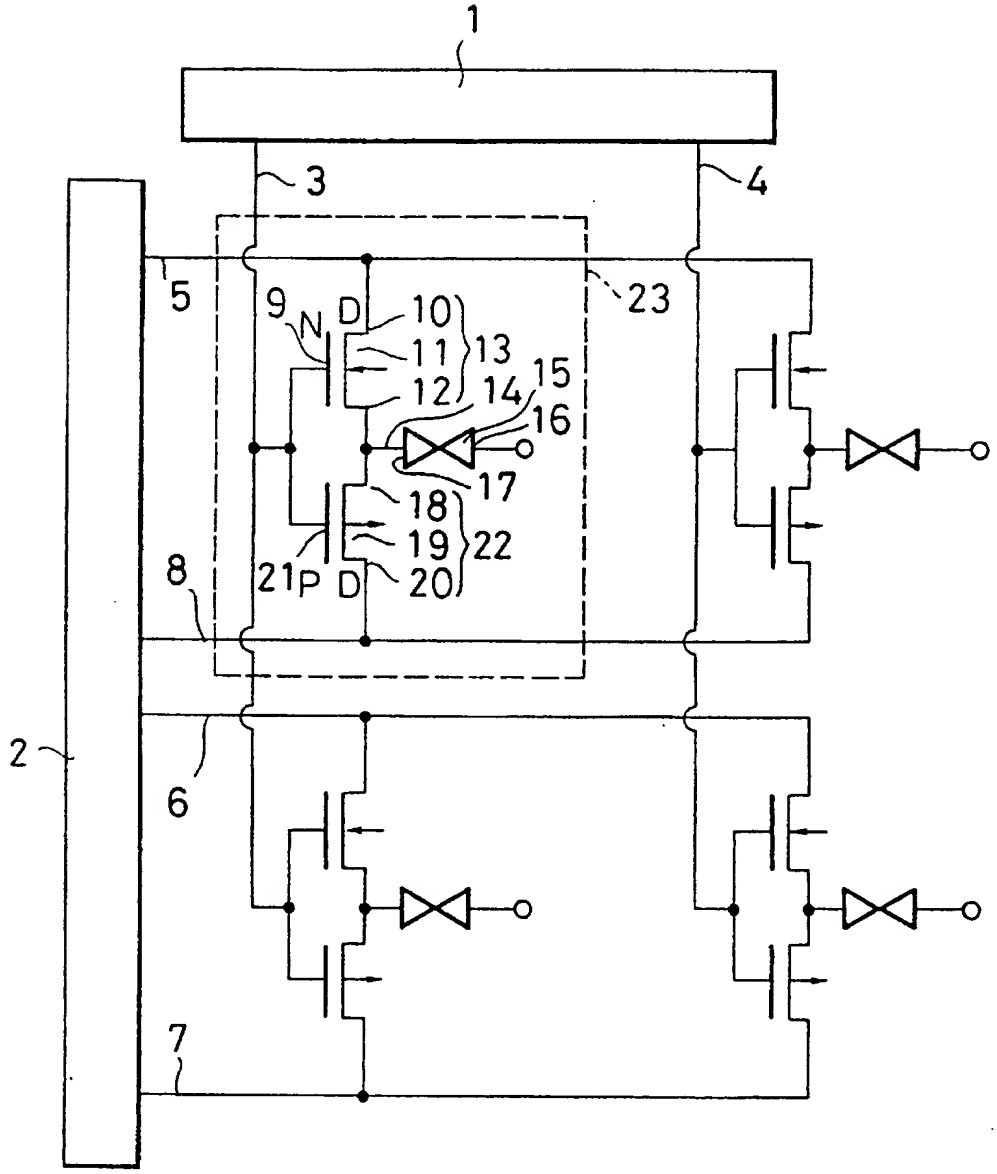


FIG. 2

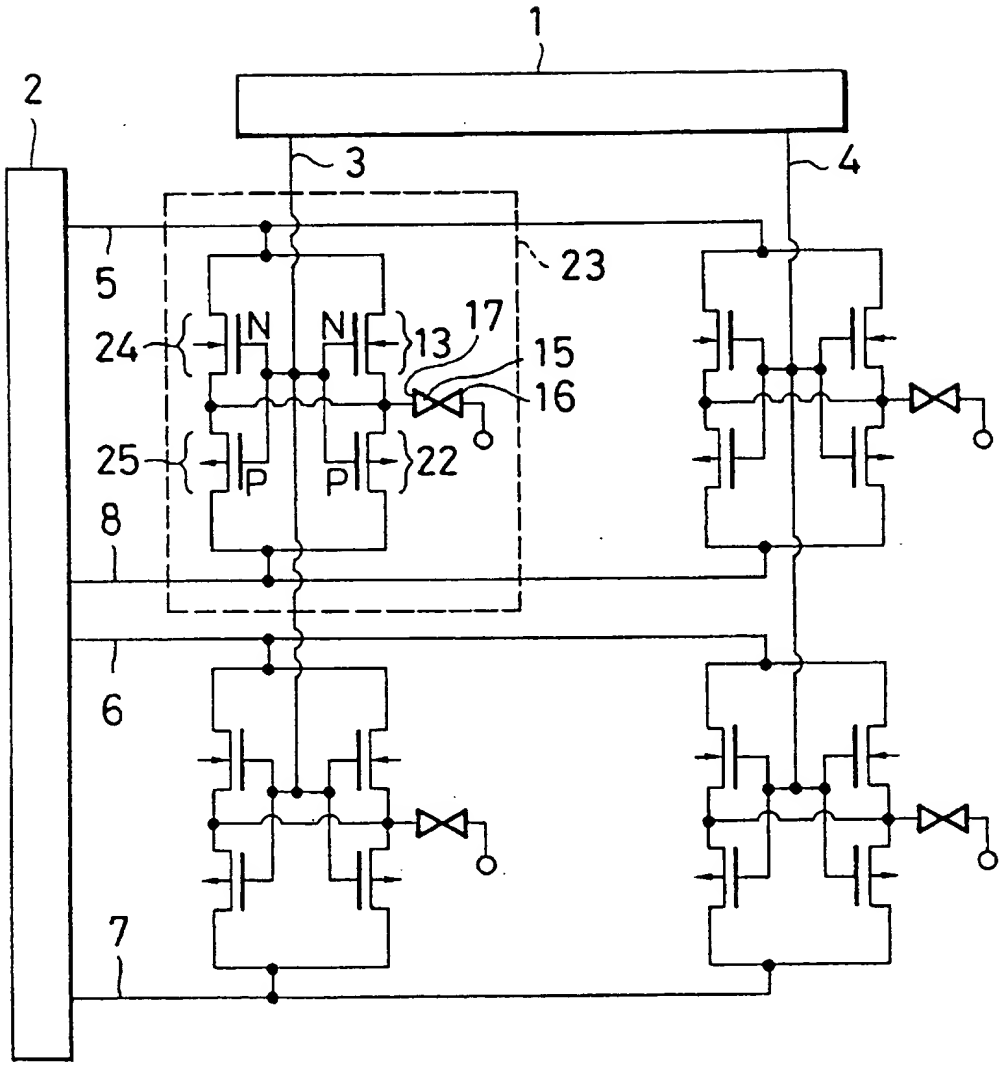


FIG. 3

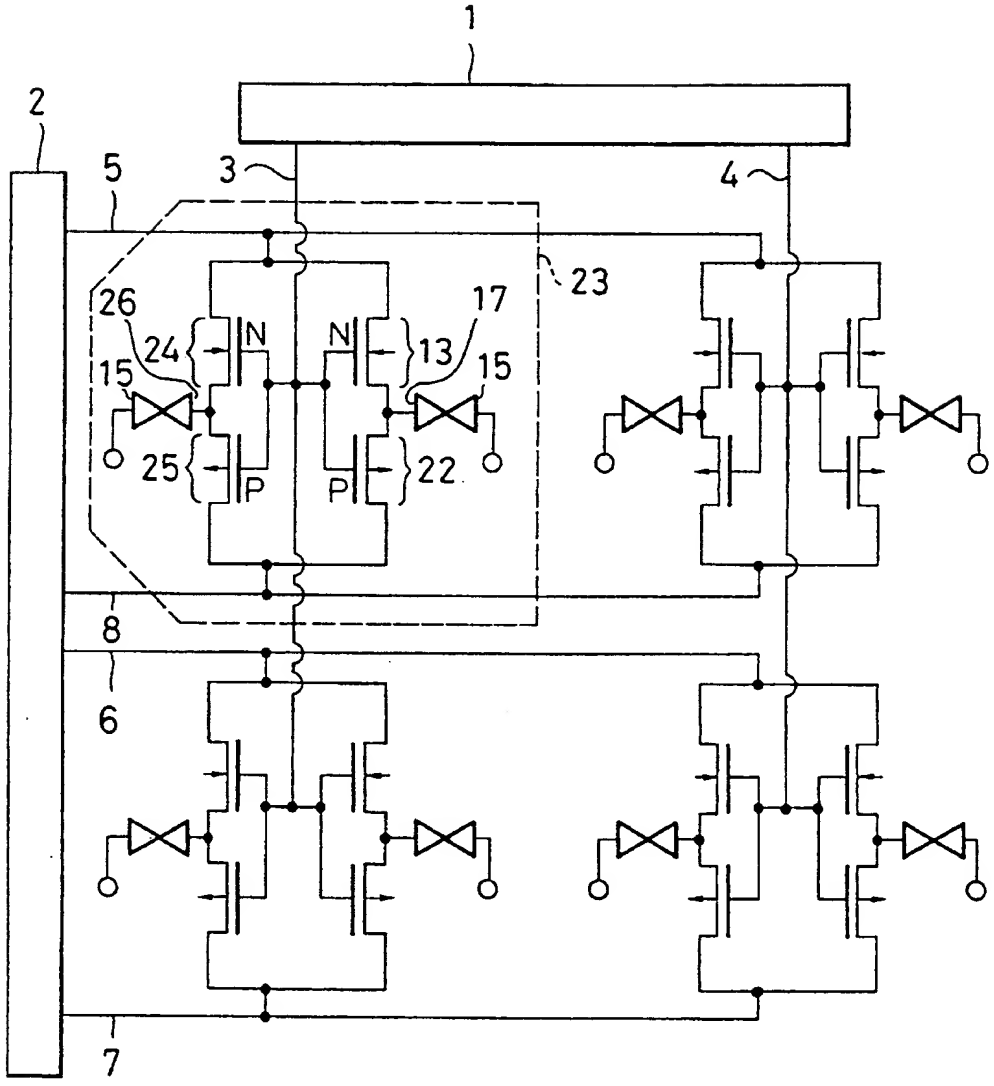


FIG. 4

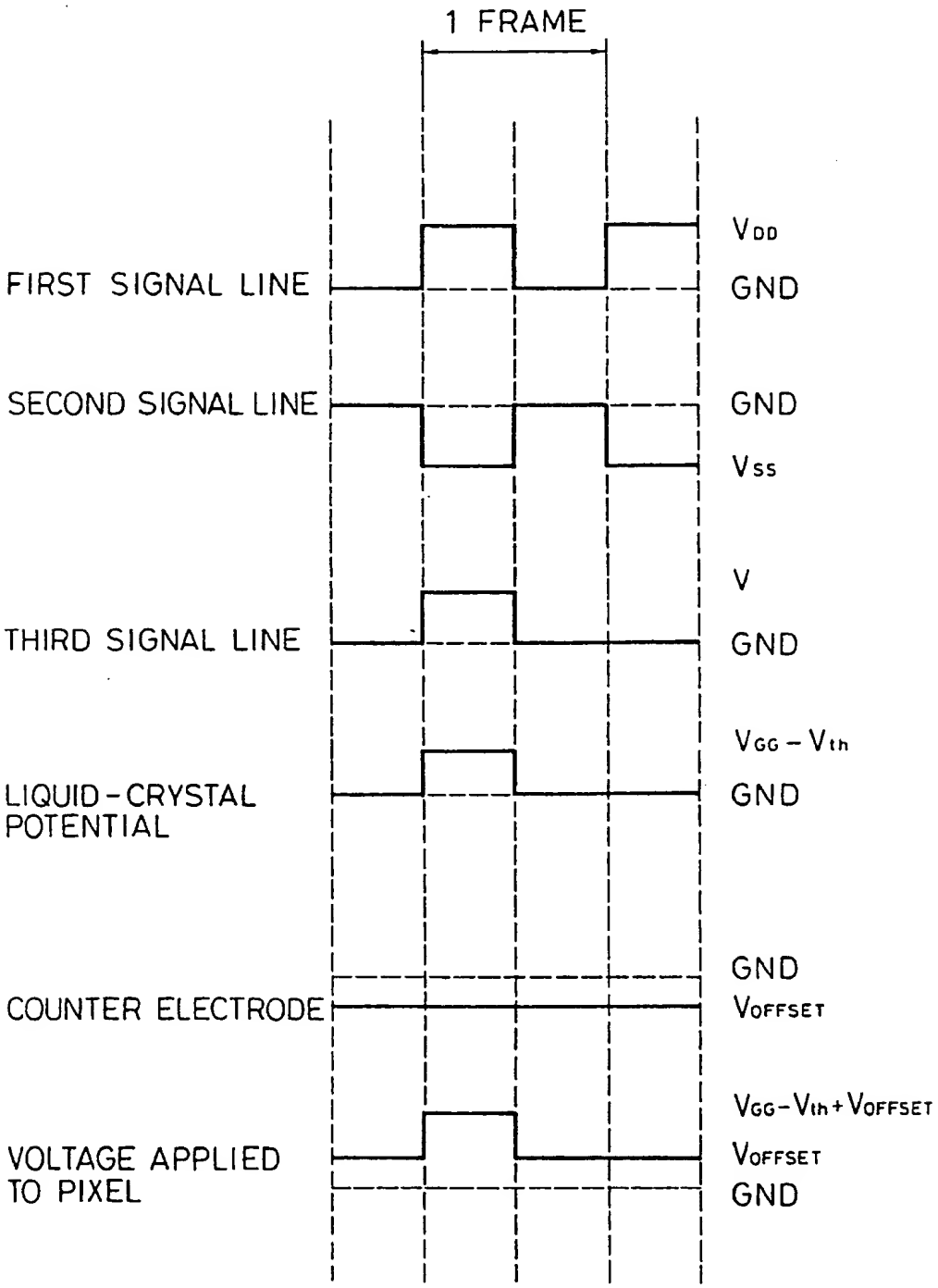

1 FRAME
FIRST SIGNAL LINE
SECOND SIGNAL LINE
THIRD SIGNAL LINE
LIQUID-CRYSTAL POTENTIAL
COUNTER ELECTRODE
VOLTAGE APPLIED TO PIXEL
VDD
GND
GND
VSS
V
GND
VGG - Vth
GND
GND
VOFFSET
VGG-Vth+VOFFSET
VOFFSET
GND

FIG. 5

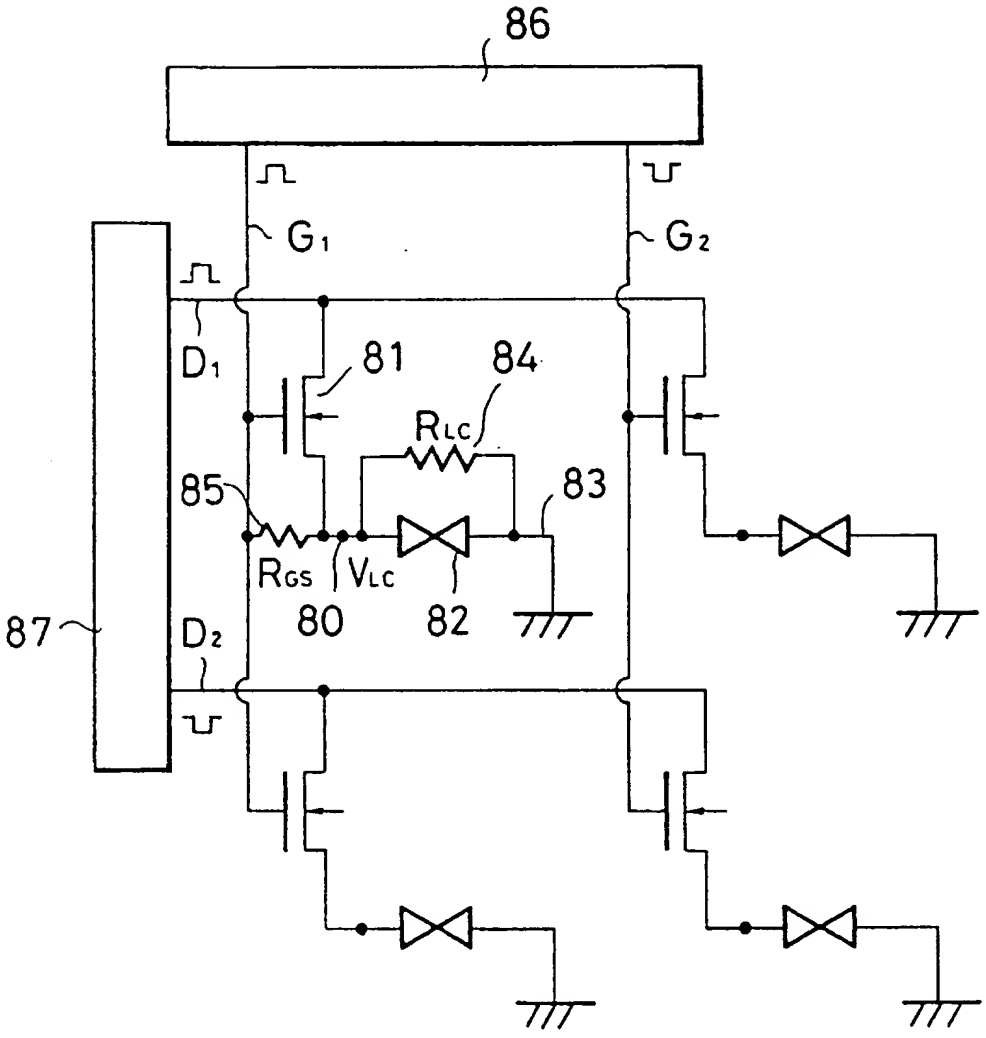


FIG. 6

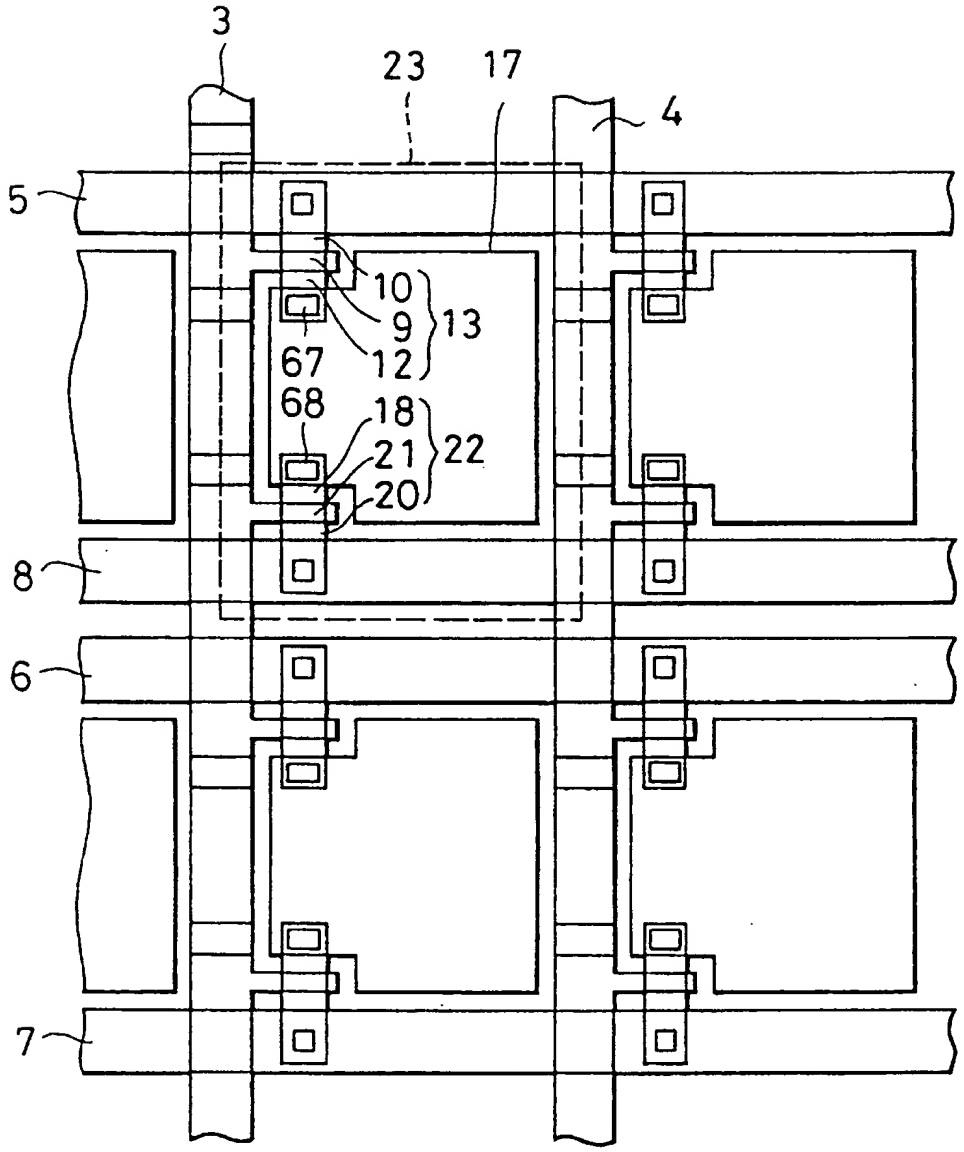


FIG. 7

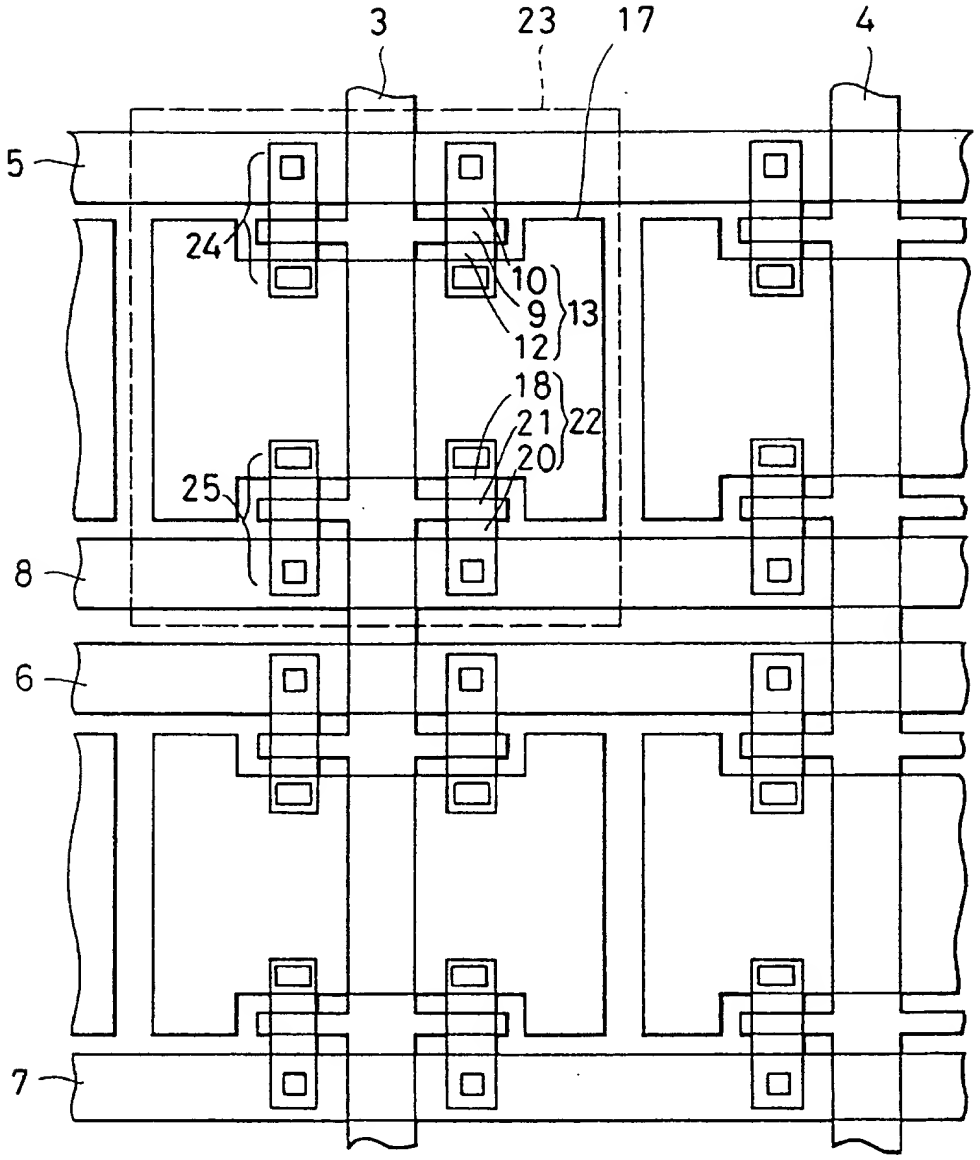


FIG 8

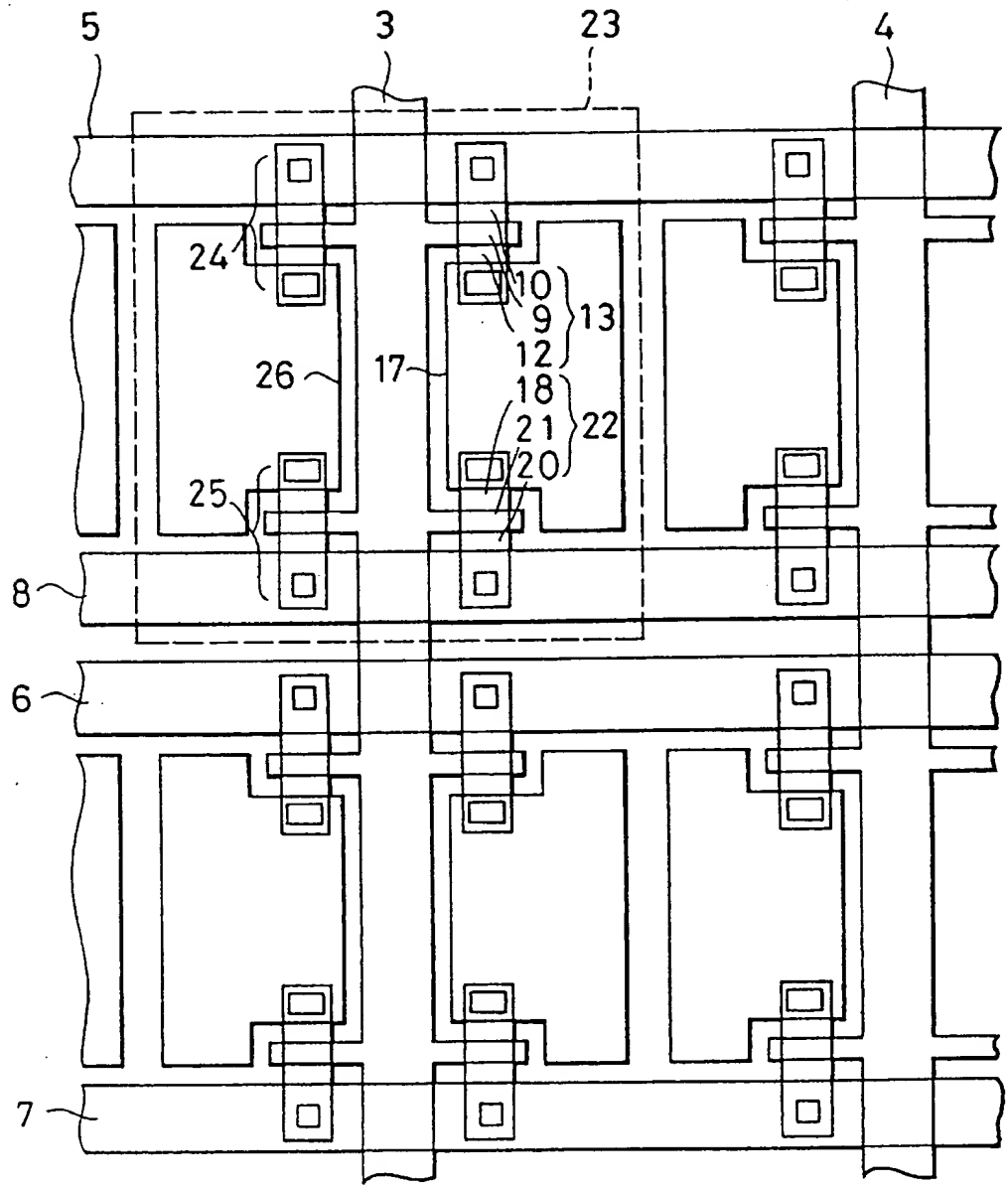
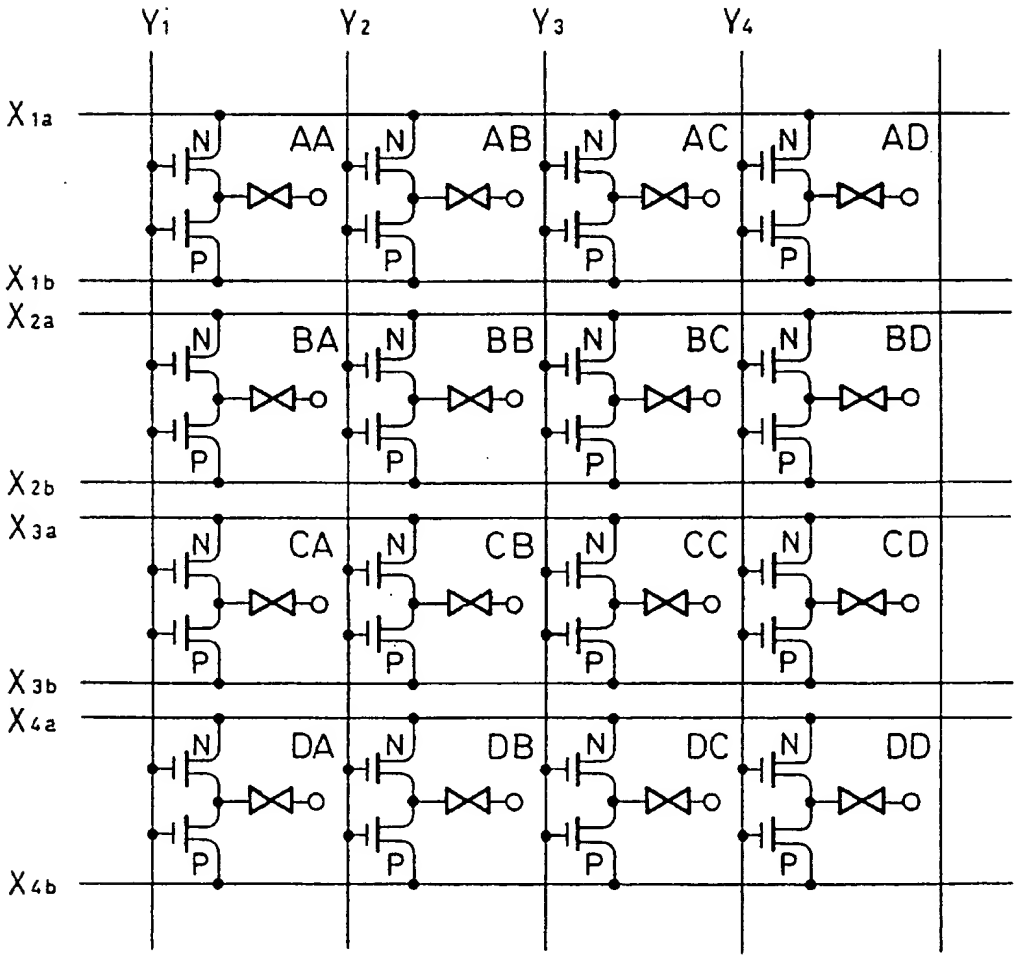


FIG. 9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X1b
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X2b
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X4a
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BB
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BD
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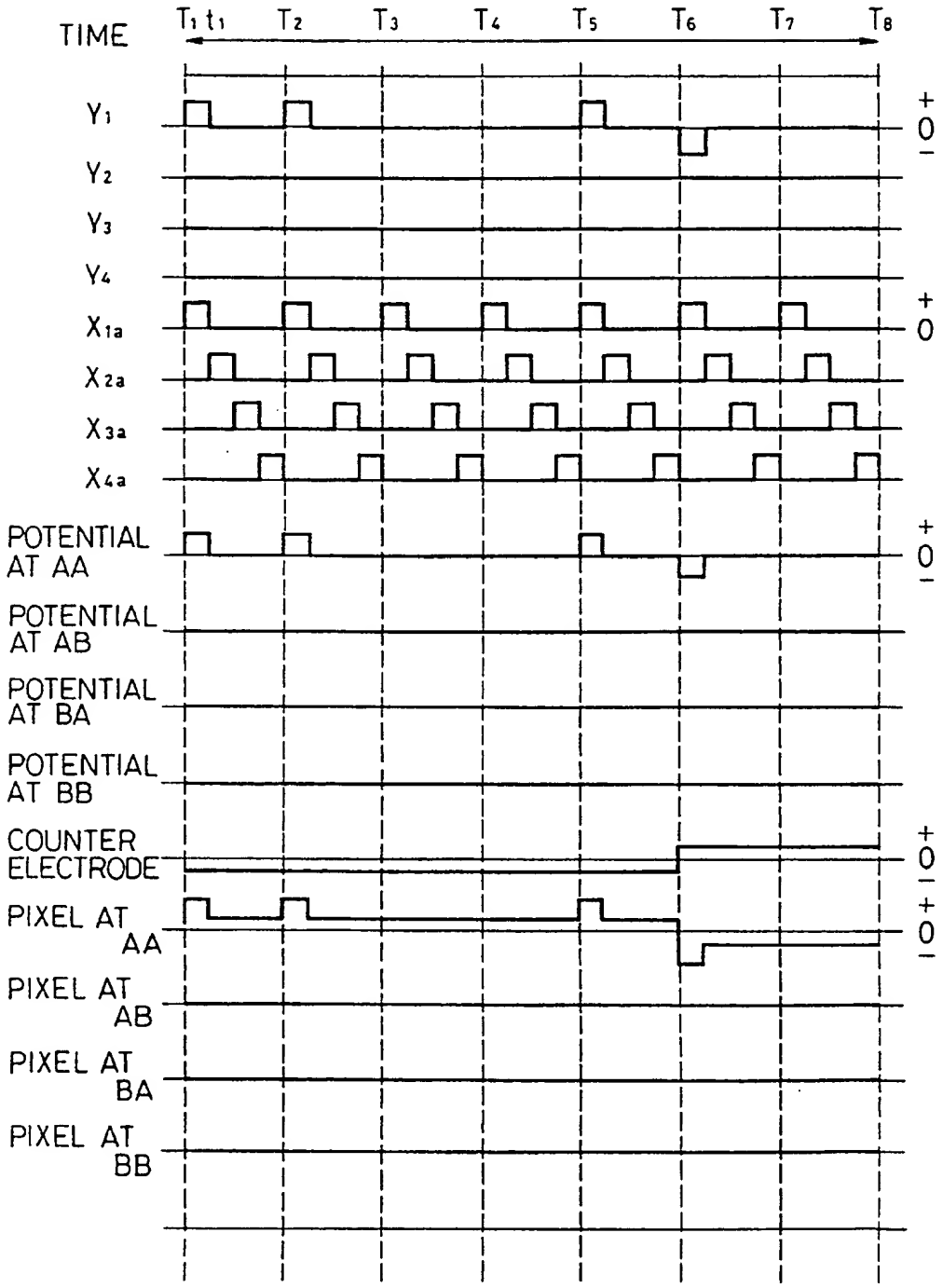
CD
DA
DB
DC
DD

FIG. 10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Y2
Y3
Y4
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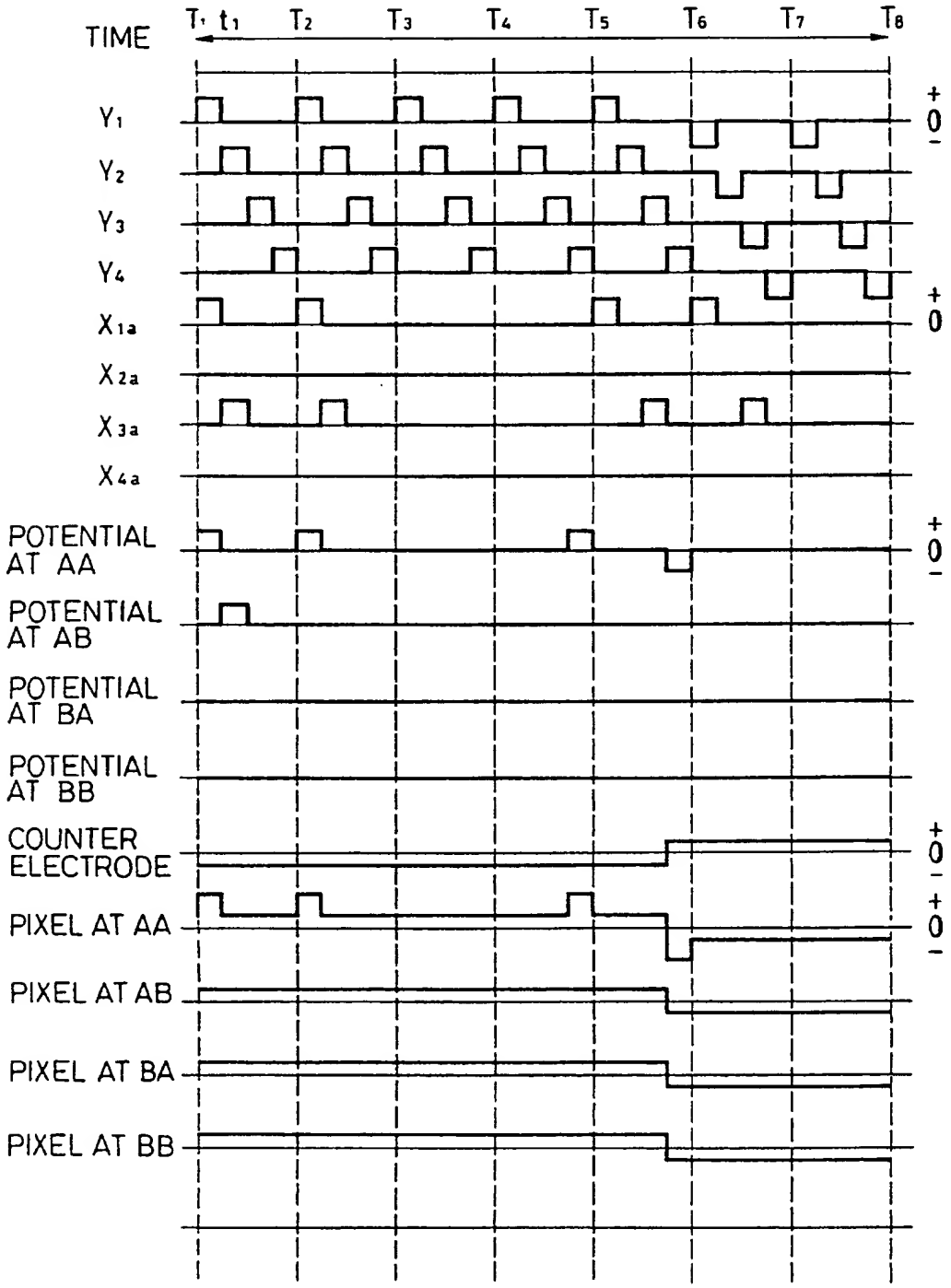
X3a
X4a
POTENTIAL AT AA
POTENTIAL AT AB
POTENTIAL AT BA
POTENTIAL AT BB
COUNTER ELECTRODE
PIXEL AT AA
PIXEL AT AB
PIXEL AT BA
PIXEL AT BB
+
0
−

FIG.11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Y2
Y3
Y4
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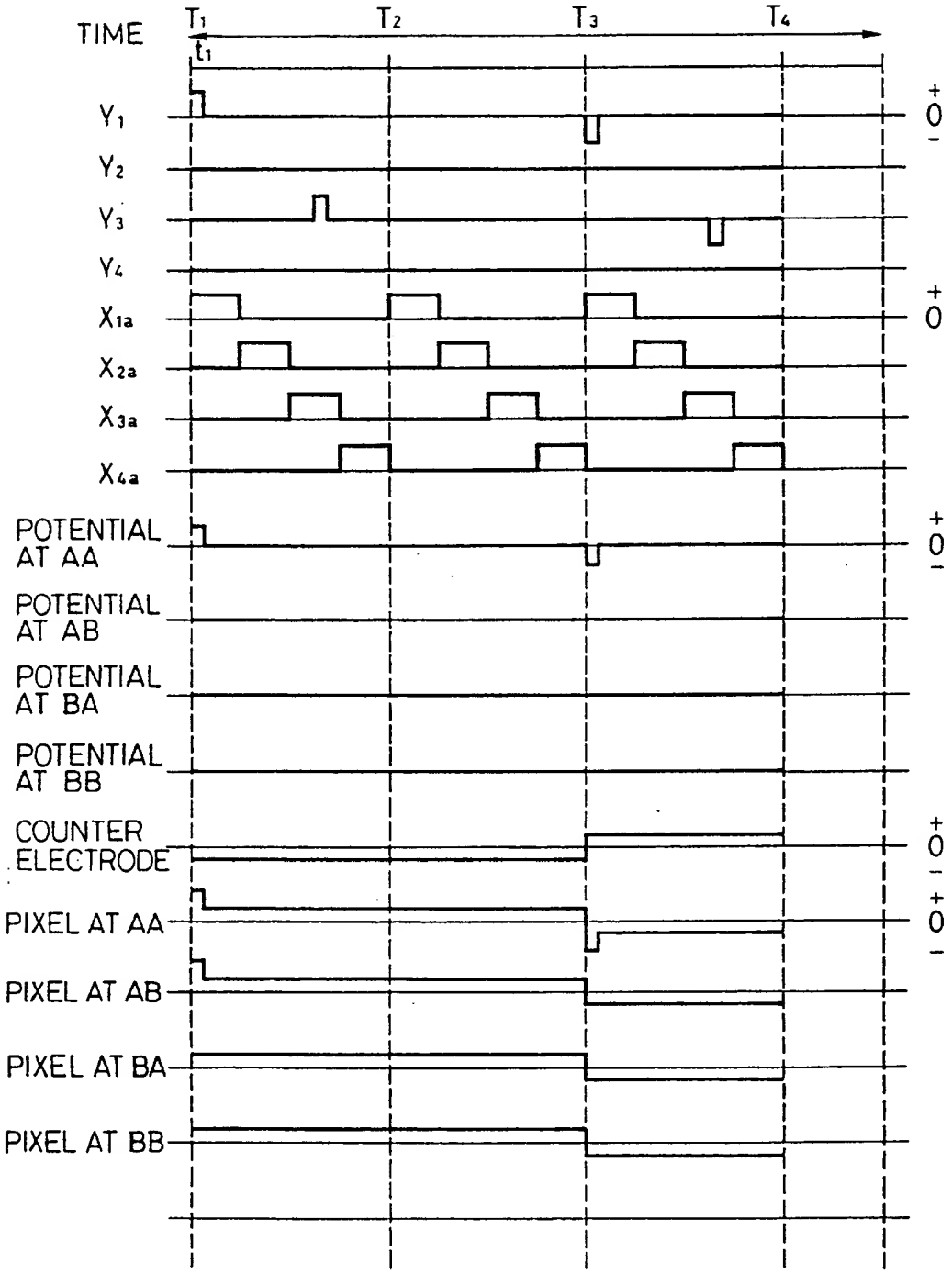
X4a
POTENTIAL AT AA
POTENTIAL AT AB
POTENTIAL AT BA
POTENTIAL AT BB
COUNTER ELECTRODE
PIXEL AT AA
PIXEL AT AB
PIXEL AT BA
PIXEL AT BB
+
0
−

FIG. 12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T4
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Y2
Y3
Y4
X1a
X2a
X3a
X4a
POTENTIAL AT AA
POTENTIAL AT AB
POTENTIAL AT BA
POTENTIAL AT BB
COUNTER ELECTRODE
PIXEL AT AA
PIXEL AT AB
PIXEL AT BA
PIXEL AT BB
+
0
−

FIG.13(A)

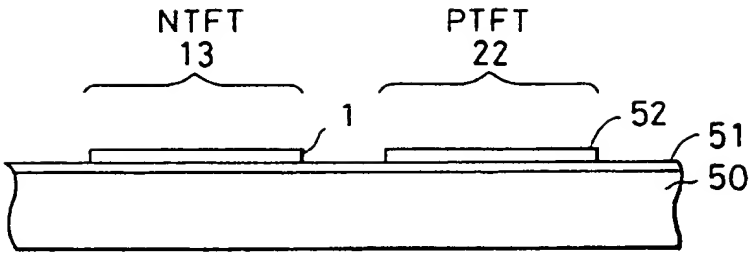


FIG.13(B)

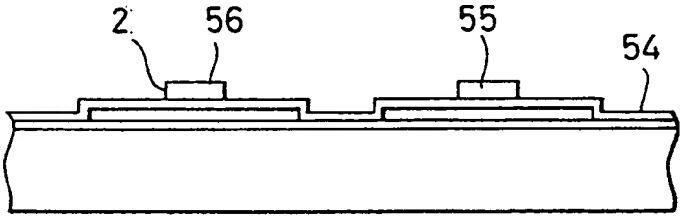


FIG.13(C)

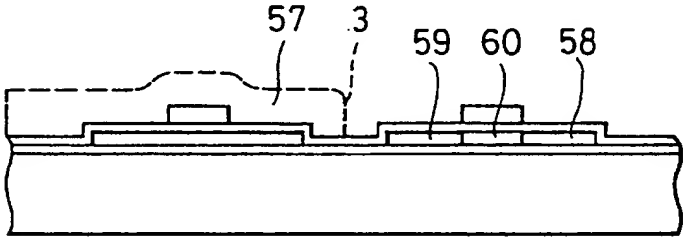


FIG.13(D)

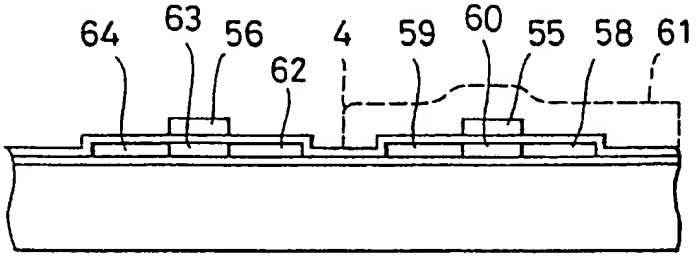


FIG.13(E)

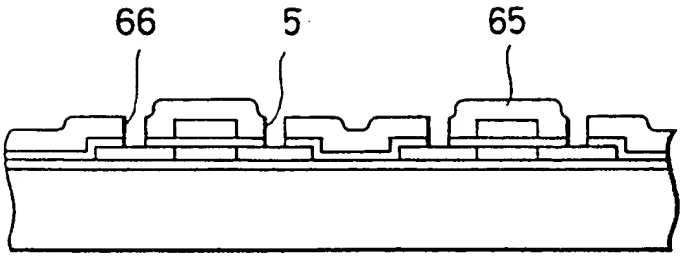


FIG.13(F)

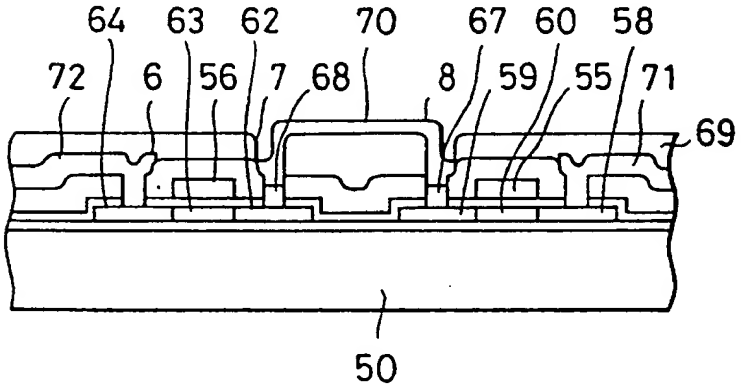


FIG. 14

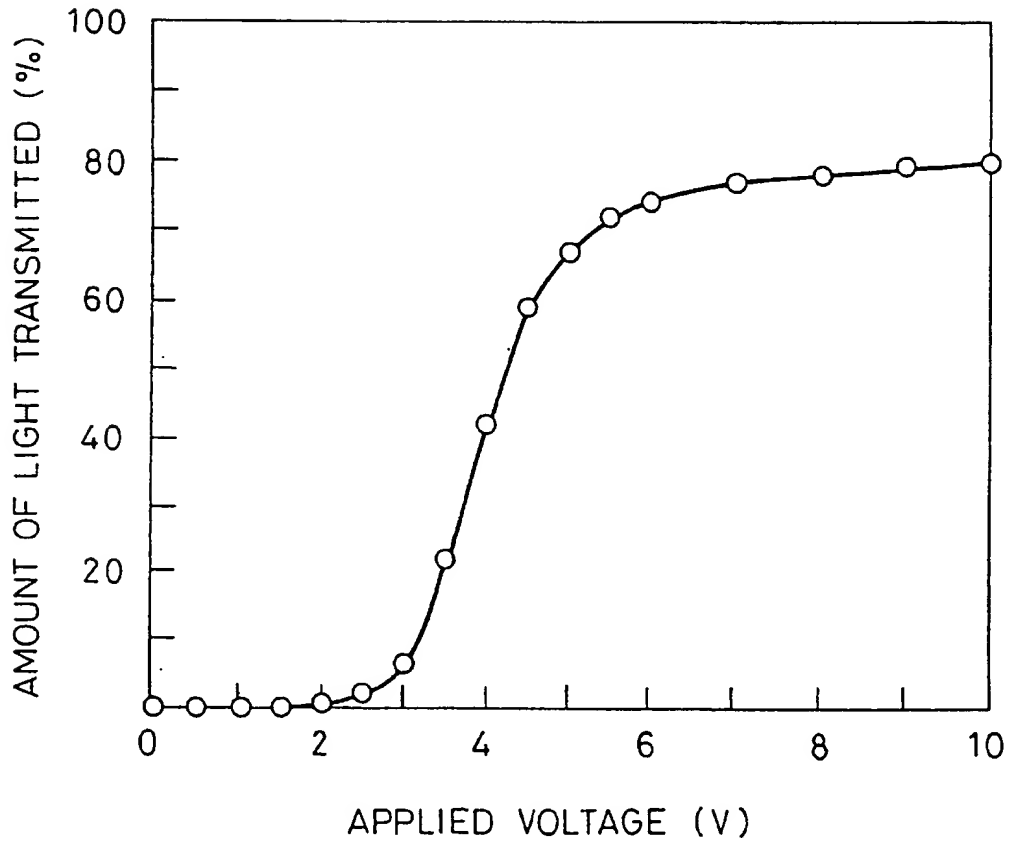

AMOUNT OF LIGHT TRANSMITTED (%)
100
80
60
40
20
0
2
4
6
8
10
APPLIED VOLTAGE (V)

FIG.15

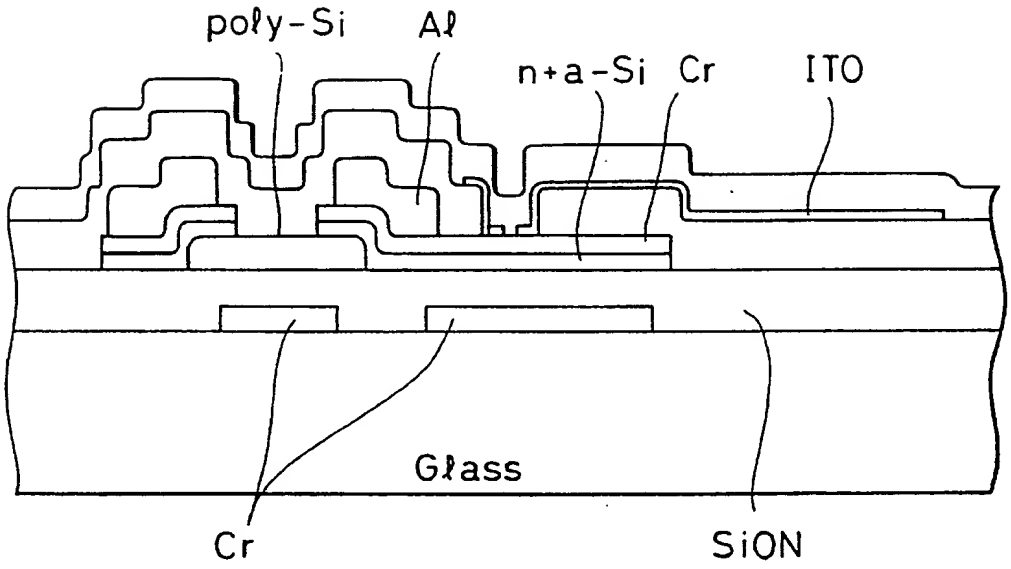


FIG.16

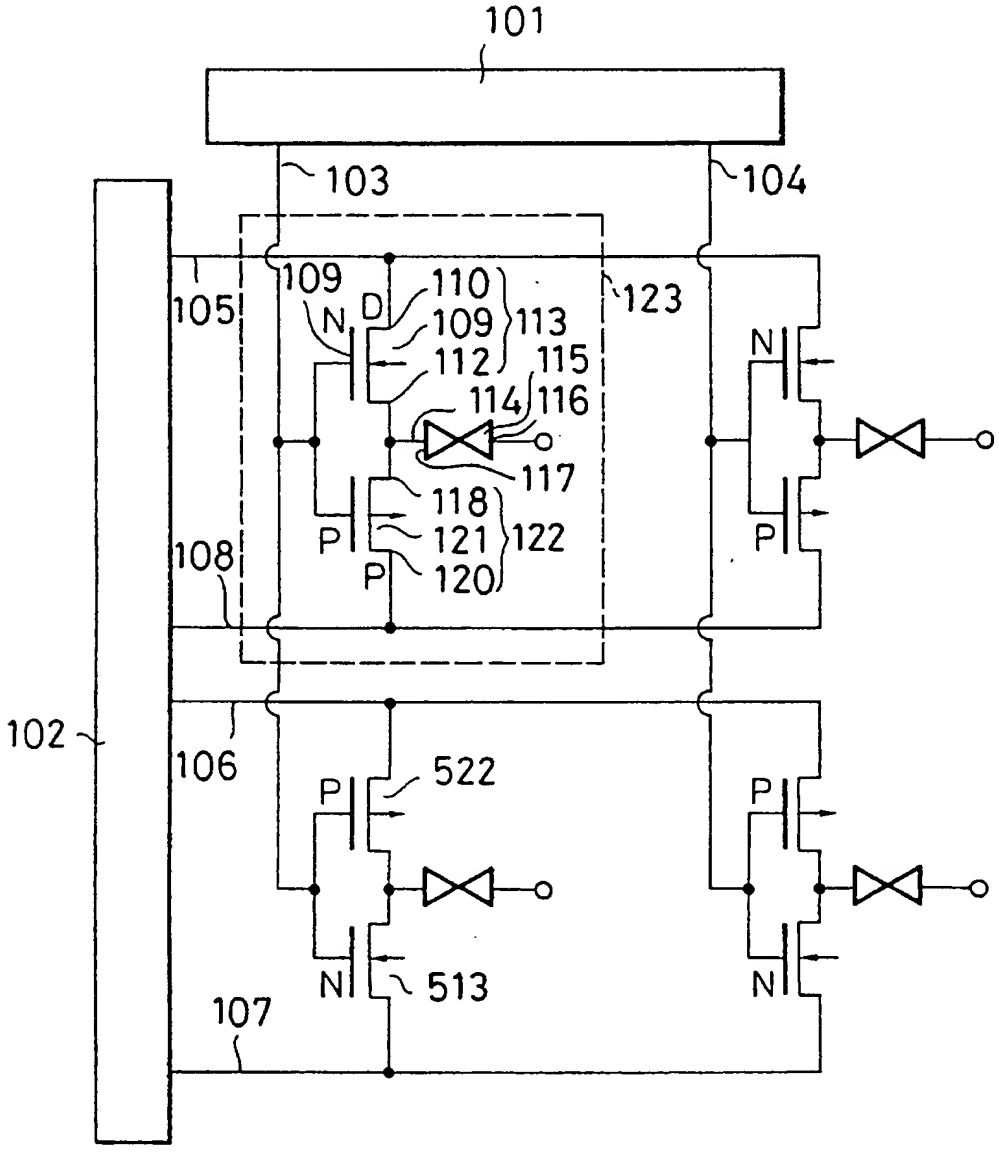

101
103
104
105
109
110
113
123
N
D
109
112
115
114
116
117
118
121
122
P
120
108
102
106
522
513
107

FIG.17

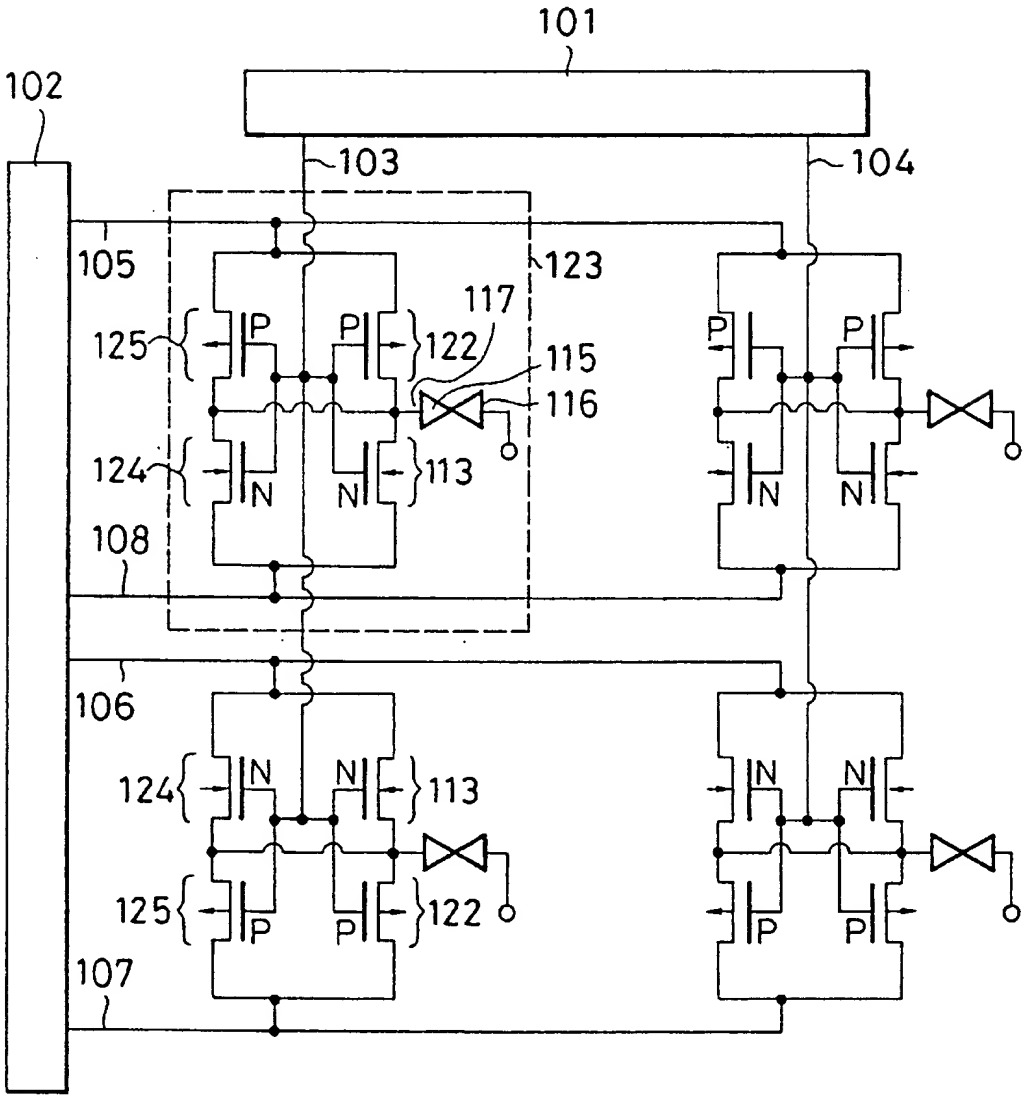

101
102
103
104
105
123
117
125
P
P
122
115
116
124
N
N
113
108
106
124
N
N
113
125
P
P
122
107

FIG.18

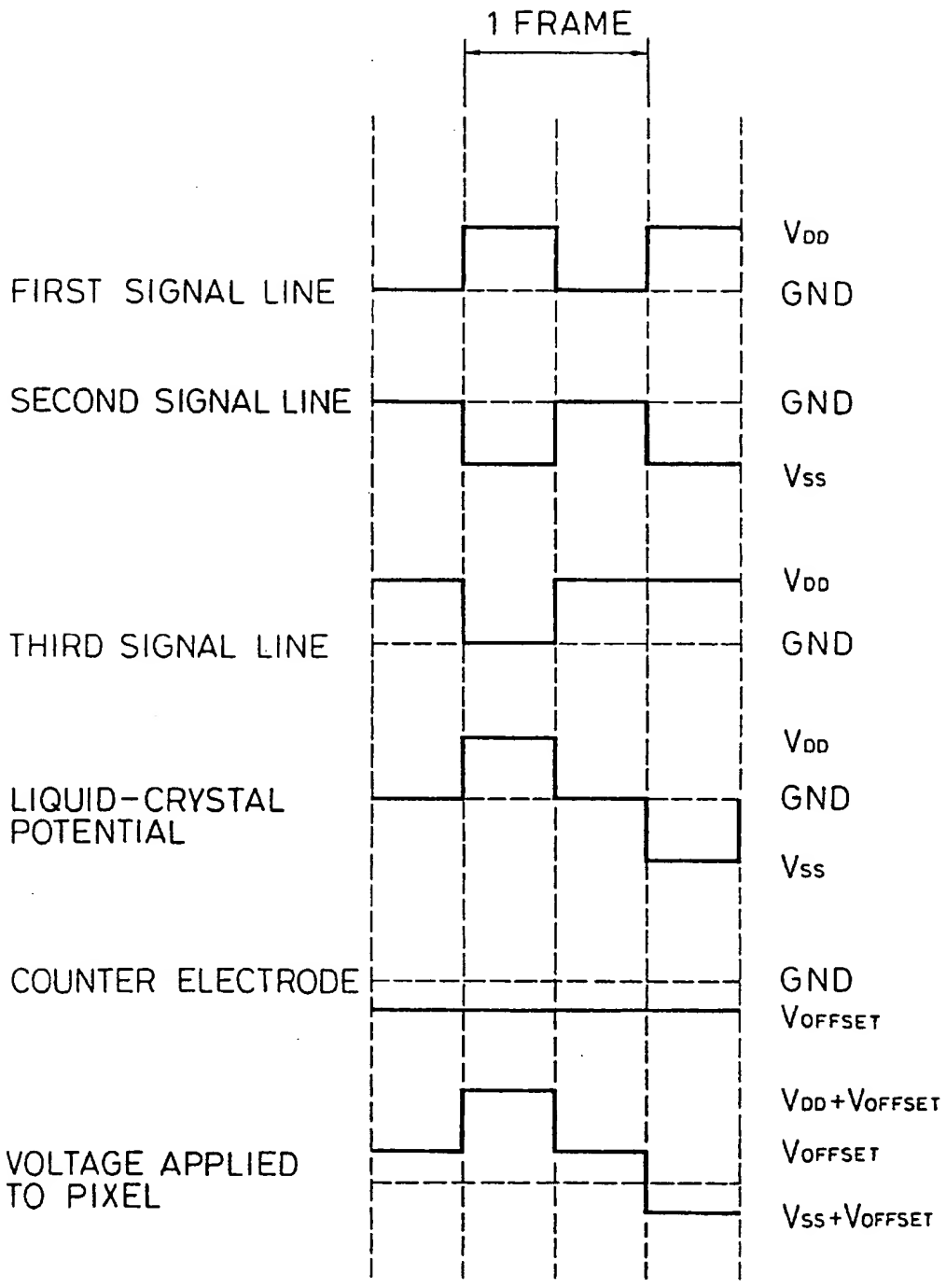

1 FRAME
FIRST SIGNAL LINE
SECOND SIGNAL LINE
THIRD SIGNAL LINE
LIQUID-CRYSTAL POTENTIAL
COUNTER ELECTRODE
VOLTAGE APPLIED TO PIXEL
VDD
GND
VSS
VOFFSET
VDD+VOFFSET
VSS+VOFFSET

FIG.19

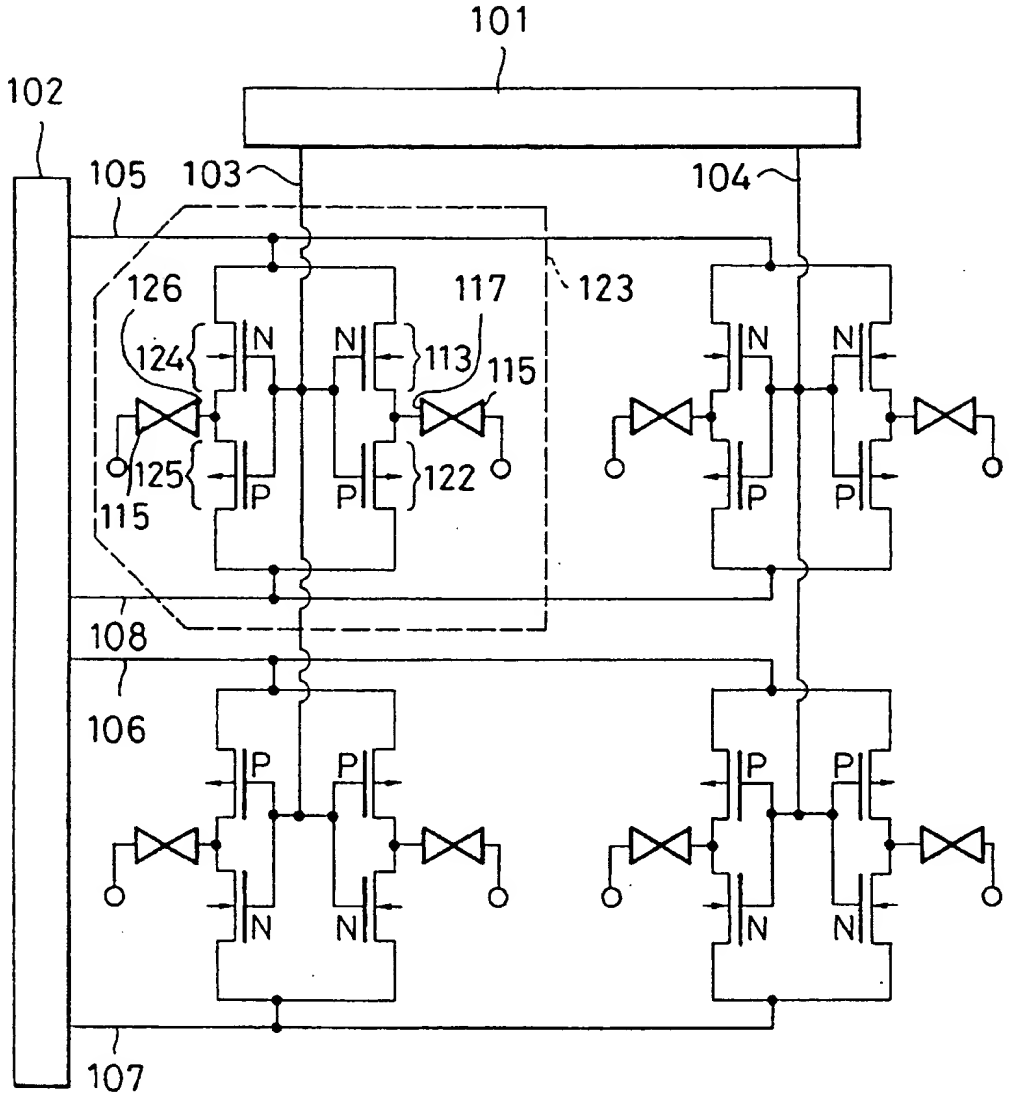

101
102
105
103
104
126
117
123
124
N
N
113
115
125
P
P
122
115
108
106
P
P
N
N
107

FIG. 20

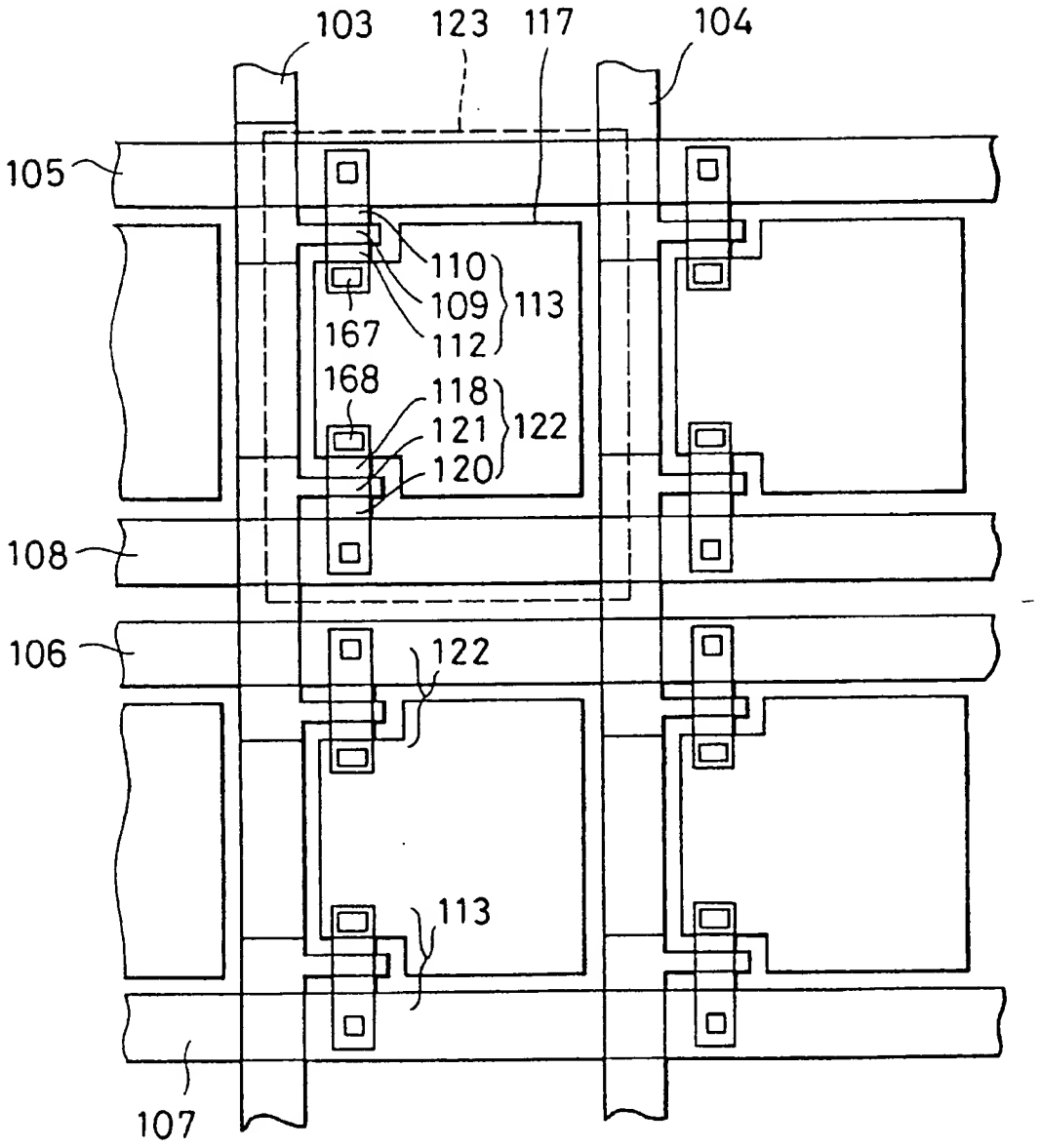

103
123
117
104
105
110
109
112
113
167
168
118
121
120
122
108
106
122
113
107

FIG. 21

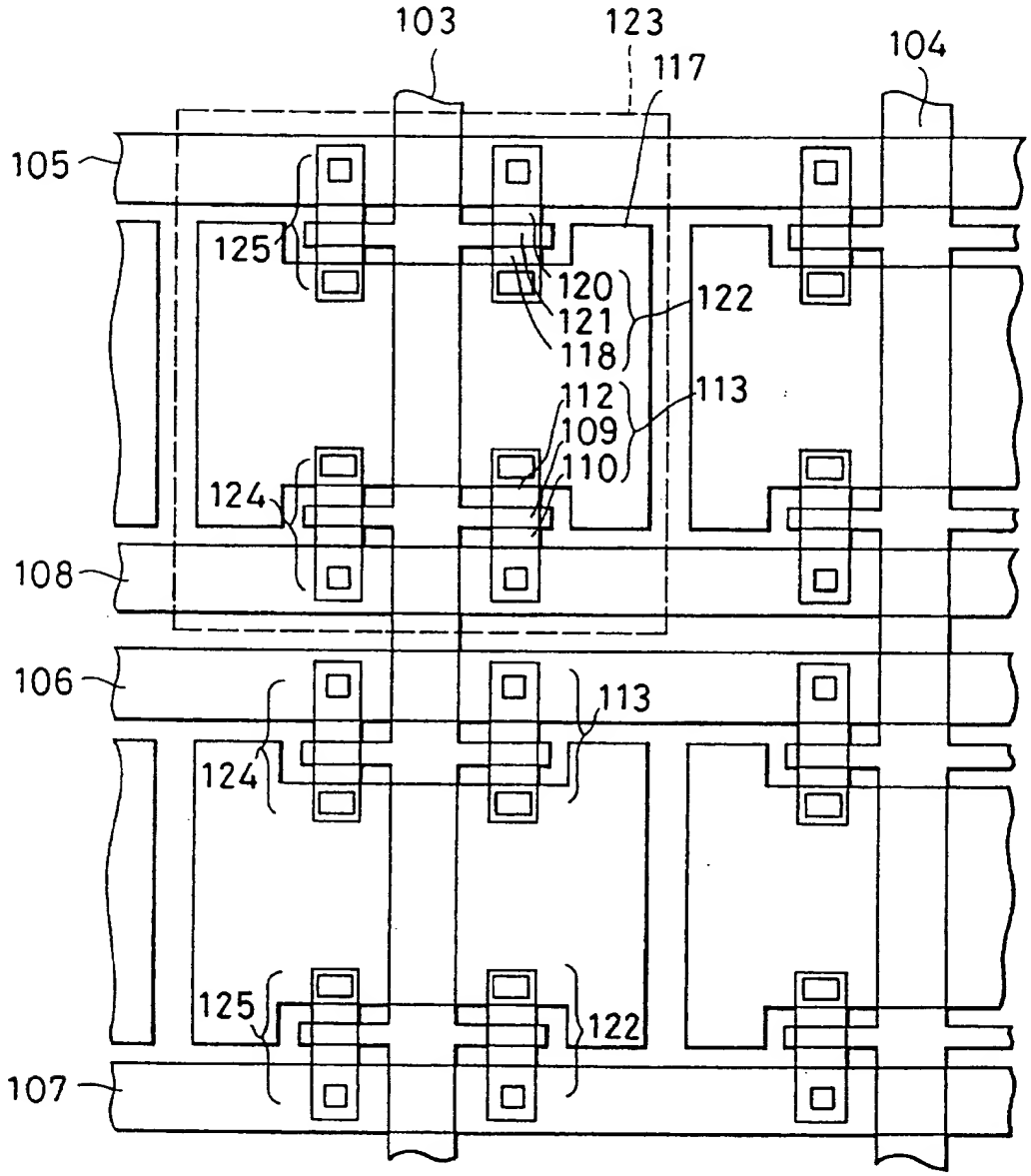
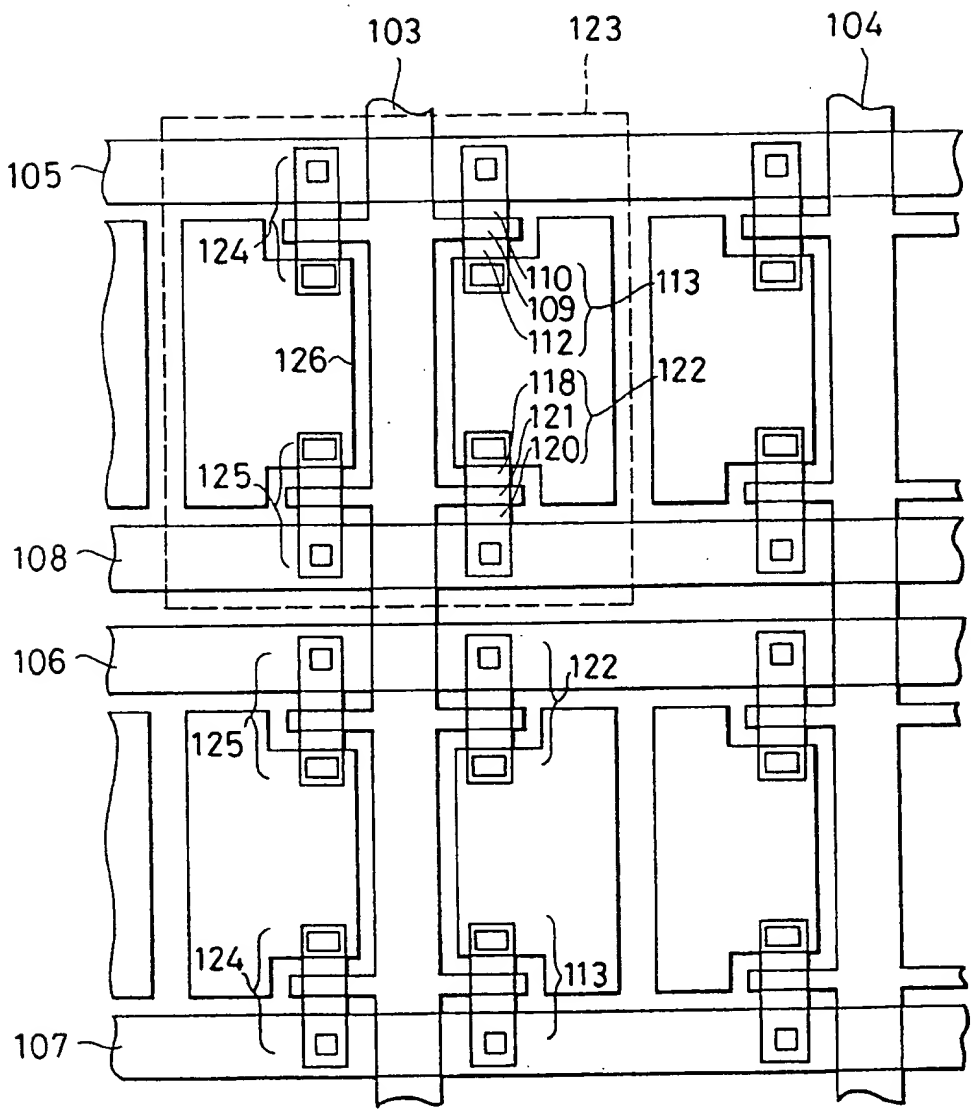

103
123
117
104
105
125
120
121
118
122
112
109
110
113
124
108
106
113
124
125
122
107

FIG. 22


103
123
104
105
124
110
109
112
113
126
118
121
120
122
125
108
106
122
125
124
113
107

ELECTRO-OPTICAL DEVICE AND METHOD OF DRIVING THE SAME

This is a divisional application of Ser. No. 08/104,935 filed Aug. 12, 1993, now U.S. Pat. No. 5,383,041, which itself is a continuation of Ser. No. 07/805,521, filed Dec. 13, 1991, now abandoned.

FIELD OF THE INVENTION

The present invention relates to an electro-optical device and, more particularly, to a liquid crystal electro-optical device comprising thin-film transistors. It also relates to a method of driving an electro-optical device.

BACKGROUND OF THE INVENTION

Known liquid crystal electro-optical devices are TN type liquid crystal electro-optical devices using nematic liquid crystals, STN type liquid crystal electro-optical devices using nematic liquid crystals, ferroelectric liquid crystal electro-optical devices, and dispersion liquid crystal electro-optical devices. In a dispersion liquid crystal electro-optical device, a liquid crystal layer comprising a nematic, cholesteric, or smectic liquid crystal dispersed in a solid-phase polymer is sandwiched between a pair of substrates. The sandwiched liquid crystal is maintained in a particulate or spongy state. A known method of forming this liquid crystal layer consists in dispersing the liquid crystal in the polymer and shaping the polymer into a thin film on a substrate or a film. The liquid crystal is dispersed in the polymer by encapsulating the liquid crystal in a material. Materials which have been proposed as encapsulating materials include gelatin, gum arabic, and polyvinyl alcohol.

In these techniques, those liquid crystal molecules which are encapsulated in polyvinyl alcohol and exhibit a positive dielectric anisotropy in a thin film are lined up in the direction of the electric field in the presence of this field. If the liquid crystal is identical in refractive index to the polymer, transparency appears. On the other hand, where there exists no electric field, the molecules of the liquid crystal do not line up in a given direction; rather they are oriented randomly. Therefore, the liquid crystal differs in refractive index from the polymer. The incident light is scattered, and transmission of the light is hindered. In this state, the device appears white and cloudy. In this way, the encapsulated liquid crystal molecules are dispersed in a thin film polymer. Some structures are known other than the above structure. For example, in one structure, a liquid crystal material is dispersed in epoxy resin. Another structure utilizes phase separation between a liquid crystal and a photocurable substance. In a further structure, a liquid crystal is immersed in polymeric molecules which are bonded together in three dimensions. These liquid crystal electro-optical devices are herein collectively referred to as dispersion liquid crystal electro-optical devices.

One of the factors which determine the properties of a dispersion liquid crystal electro-optical device is the degree of dispersion in the region where the liquid crystal exists. In particular, in the structure comprising encapsulated liquid crystal molecules, the determining factor is the degree of dispersion of the capsules. In the structure using a polymer, the factor is the degree of dispersion of spatial portions. Where their uniformity is not good, the average electro-optical property of the liquid crystal material does not show steepness. Hence, the threshold value for activating the device is not fixed. A typical example of electro-optical properties of dispersion liquid crystals is shown in FIG. **14**.

One method for solving this problem is to determine the threshold value, using thin film transistors (TFTs), called active devices. Also, this method is indispensable. Usually, n-channel TFTs are used in dispersion liquid crystal devices. Where only one kind of n-channel and p-channel TFTs is used to activate the device, it is impossible to sufficiently suppress the leakage current in off state. Therefore, it is necessary to form independent capacitive elements parallel with the capacitive components of the liquid-crystal element. FIG. **15** shows the structure of a typical liquid crystal device using TFTs of a single channel.

It is known that active liquid crystal electro-optical devices using TFTs have excellent performance. The TFTs are fabricated from an amorphous or polycrystalline semiconductor. One pixel is formed by a thin-film transistor of one conductivity type, i.e., either p- or n-type. Generally, an n-channel thin film transistor (NTFT) is connected in series with each pixel electrode. A typical example is shown in FIG. **5**.

Generally, an active-matrix, liquid crystal electro-optical device has very numerous pixels, for example, 480×640 or 1260× 960. To simplify the illustration, a matrix arrangement of 2× 2 is shown in FIG. **5**, where plural gate lines G_1 and G_2 and plural signal lines D_1 and D_2 are arranged so as to intersect each other. Pixel elements are installed at the intersections. Each pixel element comprises a liquid crystal portion **82** and a thin film transistor (TFT) portion **81**. Signals are applied to the pixel elements from peripheral circuits **88** and **87** to selectively activate the pixels, for providing desired display.

However, where this liquid crystal electro-optical device is manufactured in practice and a display is provided, the output voltage V_{LC} **80** from each TFT, or the input voltage to the liquid crystal, frequently does not go high when it should go high. Conversely, when it should go low, it often fails to go low. This is because the characteristic of each switching device applying a signal to a pixel electrode lacks symmetry. Specifically, the electrical characteristic of the charging to each pixel electrode is different from the electrical characteristic of the discharging from the electrode. Intrinsically, the liquid crystal **82** is insulative in operation. When the TFT is not conducting, the liquid-crystal potential V_{LC} is in a floating condition. Since the liquid crystal **82** is equivalently a capacitor, the potential V_{LC} is determined by the electric charge stored in it. Leakage of this electric charge takes place where the liquid crystal takes a comparatively small resistance of R_{LC}, where dust or impurity ions exist, or where a resistance R_{GS} **85** is formed because of pinholes in the gate insulating film of each TFT. Under this condition, the potential V_{LC} does not take an intended value. Consequently, a high production yield cannot be achieved for a liquid crystal electro-optical device comprising one panel having 200 thousand to 5 million pixels.

Where a twisted nematic liquid crystal is used as the liquid crystal **82**, a rubbed orientation film is formed on each electrode to orientate the liquid crystal. During the rubbing, static electricity is produced. This causes a weak dielectric breakdown. As a result, leakage takes place between adjacent pixels or conductors. Also, leakage occurs where the gate insulating film is weak.

It is quite important for an active liquid crystal electro-optical device that the liquid-crystal potential, or the input voltage to the liquid crystal, be maintained at the given initial value during one frame. In practice, however, active

devices often malfunction. The practical situation is that the liquid-crystal potential is not always retained at the initial value during one frame.

When the liquid crystal is driven by supplying a signal thereto, if a large amount of one of positive voltage and negative voltage is applied to the liquid crystal as compared with the other, then electrolysis occurs, attacking or denaturing the liquid crystal material. In consequence, a satisfactory display cannot be provided. In order to solve such a problem, an AC signal is supplied. However, this AC signal is quite complex.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide an electro-optical device which has a larger current margin, hence high response speed, and in which the input voltage applied to each pixel electrode, or the liquid crystal potential V_{LC}, is sufficiently stably maintained either at 1 (high state) or 0 (low state) such that the level of the potential does not drift during one frame.

It is another object of the invention to provide a dispersion liquid crystal electro-optical device which has wide substrates, and in which desired threshold values are secured by the action of active elements to compensate for nonuniform dispersion of liquid crystal molecules.

The foregoing objects of the present invention are achieved by an electro-optical device comprising:

a pair of substrates at least one of which is transparent;

a liquid crystal layer disposed between said substrates, said layer comprising a transparent solid and a material comprising a liquid crystal; and

at least one pixel,

wherein said one pixel is provided with complementary transistors comprising an n-channel transistor and a p-channel transistor provided on an inside of one of said substrates;

an electrode provided on said inside of one of said substrates and connected to one of drain and source terminals of said n-channel transistor and one of drain and source terminals of said p-channel transistor;

a pair of row control lines one of which is connected to the other one of the drain and source terminals of said n-channel transistor and the other one of which is connected to the other one of the drain and source terminals of said p-channel transistor; and

a column control line connected to gate terminals of said n-channel transistor and said p-channel transistor.

In the operation of the electro-optical device, an electric signal is applied to said row control lines and an electric signal is applied to said column control line for the duration of the electric signal applied to said row control lines to drive the complementary TFTs. Thus, the pixels constituting the electro-optical device are selectively made to go on or go out.

Other objects and features of the invention will appear in the course of the description thereof which follows.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit diagram of an active display device using complementary thin film transistors (TFTs) in accordance with the present invention;

FIG. 2 is a circuit diagram of another active display device using complementary thin film transistors (TFTs) in accordance with the present invention;

FIG. 3 is a circuit diagram of a further active display device using complementary thin film transistors (TFTs) in accordance with the present invention;

FIG. 4 is a waveform diagram of signals for activating active display devices according to the invention;

FIG. 5 is a circuit diagram of the prior art active liquid crystal device;

FIG. 6 is a fragmentary plan view of one example of one substrate of the liquid crystal display shown in FIG. 1;

FIG. 7 is a fragmentary plan view of one substrate of the liquid crystal display shown in FIG. 2;

FIG. 8 is a fragmentary plan view of one example of one substrate of the liquid crystal display shown in FIG. 3;

FIG. 9 is circuit diagram of a 4×4 active liquid crystal display using complementary TFTs;

FIG. 10 is a timing chart of the waveforms of signals for driving liquid crystal displays according to the invention;

FIG. 11 is another timing chart of the waveforms of signals for driving liquid crystal displays according to the invention;

FIG. 12 is a further timing chart of the waveforms of signals for driving liquid crystal displays according to the invention;

FIGS. 13(A) to 13(F) are cross-sectional views illustrating steps for manufacturing complementary TFTs used in a liquid crystal display according to the invention;

FIG. 14 is a graph showing the electro-optical characteristic of the prior art dispersion liquid crystal;

FIG. 15 is a vertical cross section of a liquid crystal electro-optical device using the prior art TFTs;

FIG. 16 is a circuit diagram of an active display device using complementary TFTs according to the invention;

FIG. 17 is a circuit diagram of an active display device using complementary TFTs according to the invention;

FIG. 18 is a waveform diagram of signals used to drive active display devices according to the invention;

FIG. 19 is a circuit diagram of an active display device using complementary TFTs according to the invention;

FIG. 20 is a fragmentary plan view of another example of one substrate of the liquid crystal display shown in FIG. 1;

FIG. 21 is a fragmentary plan view of one substrate of a liquid crystal display according to the invention; and

FIG. 22 is a fragmentary plan view of one substrate of a liquid crystal display according to the invention.

DETAILED DESCRIPTION OF THE INVENTION

Typical examples of liquid crystal electro-optical device to which the invention can be applied are shown in the circuits diagrams of FIGS. 1, 2, and 3. The layouts of actual patterns of these examples are shown in FIGS. 6, 7, and 8, respectively. To simplify the illustration, we take a matrix of 2×2 as an example. Referring to FIG. 1, the gates of n-channel TFTs (thin film transistors) and of p-channel TFTs are connected to each other. Also, the gate of each TFT is connected to a third signal line 3 or 4 which extends along the Y-axis. The common output terminal of each complementary TFT pair is connected with a liquid crystal 15. The input terminal 10 of each n-channel TFT is connected with a first one 5 or 6 of a pair of corresponding signal lines extending along the X-axis. The input terminal 20 of each p-channel TFT is connected with a second one 8 or 7 of a

pair of corresponding signal lines running along the X-axis.

In this structure of FIG. 1, when an ON signal is applied to the third signal line 3 while an ON signal is being applied between the first signal line 5 and the second signal line 8 of the signal line pair, the liquid-crystal potential (V_{LC}) 14 is equal to the voltage V_{GG} minus threshold voltage V_{th} (V_{GG}-V_{th}), the voltage V_{GG} being applied to the third signal line and the voltage V_{GG}-V_{th} being applied to the first signal line. When an OFF signal is applied to the third signal line 3 while an OFF signal is being applied between the first signal line 5, and the second signal line 8, the liquid-crystal potential (V_{LC}) 14 is earth potential (ground level). When an ON signal is not applied to the third signal line 3 while an ON signal is being applied between the first signal line 5 and the second signal line 8, the liquid-crystal potential (V_{LC}) 14 is similarly null (ground level). In this way, the liquid-crystal potential (V_{LC}) 14 is changed in response to the voltage applied to the third signal line 3. The potential difference applied to the liquid crystal can be arbitrarily varied by changing the voltage of the signal applied to this signal line.

An offset voltage (electric potential) V_{OFFSET} is applied to a counter electrode 16. The voltage actually applied to the liquid crystal 15 is V_{GG}+V_{OFFSET}-V_{th} or V_{OFFSET}. In the driving method of the invention, the offset voltage V_{OFFSET} applied to the counter electrode is varied to activate and deactivate the liquid crystal at will. The threshold value actually used for activating the liquid crystal differs among liquid crystal materials. It is possible to accommodate any arbitrary threshold value by varying the offset voltage V_{OFFSET} according to the threshold value of the liquid crystal.

When the liquid crystal is driven by supplying a signal thereto, if a large amount of one of positive voltage and negative voltage is applied to the liquid crystal as compared with the other, then electrolysis occurs, attacking or denaturing the liquid crystal material. In consequence, a satisfactory display cannot be provided. In order to solve such a problem, an AC signal is applied. In the novel driving method of the present invention, an AC signal can be very easily produced simply by inverting the polarity of the offset voltage V_{OFFSET} applied to the counter electrode and the logic, i.e., either 1 or 0, of the select signals applied to the data signal lines.

In the example of FIG. 2, an n-channel TFT 13 and a p-channel TFT 22 form a first complementary TFT pair. An n-channel TFT 24 and a p-channel TFT 25 form a second complementary TFT pair. All of the four gate electrodes of these four TFTs are connected to the third signal line 3 extending in the Y-direction. The n-channel TFTs 13 and 24 have a common input terminal which is connected to the first signal line 5 extending in the X-direction. The p-channel TFTs 22 and 25 have a common input terminal that is connected with the second signal line 8 running in the X-direction. These two complementary TFT pairs have a common output terminal connected with a pixel electrode 17 which is disposed on one side of a liquid crystal 15 of a pixel 23. If a slight leakage occurs from one of the two complementary TFT pairs, the pixel electrode can be activated, because they are in phase.

In the example of FIG. 3, two pixel electrodes 17 and 26 and two corresponding complementary TFT pairs are provided for one pixel 23. The two complementary TFT pairs have a common gate electrode to which a first input signal is applied. The input terminals of the n-channel TFTs of the same complementary TFT structure are connected with the first signal line 5, while the input terminals of the p-channel TFTs of the same complementary TFT structure are connected with the second signal line 8. Even if one of two pixel electrodes for one pixel does not operate due to a trouble such as a leakage from any TFT, the other does operate. If the operation of one pair is delayed, the other operates normally and, therefore, the defective location is not noticeable during the operation of the matrix structure.

In the liquid crystal electro-optical devices described above, a dispersion liquid crystal material can be used between the pair of substrates.

In these liquid crystal electro-optical devices, the first and second signal lines forming pairs extend in the X-direction, while the third signal lines run in the Y-direction. Thus, the signal lines are arranged in rows and columns. Complementary thin film transistors and pixel electrodes are formed at the intersections of these signal lines. The source or drain of each n-channel TFT connected with a first pixel electrode is connected with the first signal line of the corresponding signal line pair extending in the X-direction. The source or drain of each p-channel TFT connected with the first pixel electrode is connected with the second signal line of the corresponding signal line pair extending in the X-direction. The source or drain of each p-channel TFT connected with the same third signal line and connected with a second pixel electrode which neighbors the first pixel electrode is connected to the second signal line of other signal line pair extending in the X-direction. The second signal line to which the p-channel TFT for the first pixel electrode is connected is adjacent to the second signal line to which the p-channel TFT for the second pixel electrode is connected. In these display devices, only a small amount of leakage takes place between these two adjacent second signal lines and therefore various kinds of electro-optical modulating layer can be provided between the pair of substrates. The electro-optical modulating layer may comprise a twisted nematic liquid crystal, a ferroelectric liquid crystal, a dispersion liquid crystal, or a polymeric liquid crystal. The amount of leakage can be reduced, irrespective of the kind of the material used in the electro-optical modulating layer.

As described above, the signal lines for the p-channel TFTs for adjacent pixels are made to neighbor each other. It is also possible that the signal lines for the n-channel TFTs for adjacent pixels neighbor each other.

Typical examples of liquid crystal electro-optical device to which the present invention can be applied are shown in the circuit diagrams of FIGS. 16, 17, and 19. The layouts of examples of their respective actual patterns are shown in FIGS. 20, 21, and 22, respectively. To simplify the illustration, we take a matrix of 2×2 as an example. In the example of matrix of 2×2 shown in FIG. 16, the gates of n-channel and p-channel TFTs are connected to each other and also to a third signal line 103 or 104 extending in the Y-direction. Each complementary TFT pair has a common output terminal which is connected with a liquid crystal 115. The input terminal 110 of each n-channel TFT is connected to the first signal line 105 or 107 of a signal line pair extending in the X-direction. The input terminal 120 of each p-channel TFT is connected to the second signal line 108 or 106 of a signal line pair running in the X-direction.

In this structure, as shown in FIG. 4, an ON signal is applied to the third signal line 103 while an ON signal is being applied between the first signal line 105 and the second signal line 108 forming a pair. At this time, the liquid-crystal potential (V_{LC}) 114 is equal to V_{GG}-V_{th}, the voltage V_{GG} being applied to the third signal line 103 and the voltage V_{GG}-V_{th} being applied to the first signal line 105. When an OFF signal is applied to the third signal line

103 while an OFF signal is being applied between the first signal line 105 and the second signal line 108 of the pair, the liquid-crystal potential (V_{LC}) 114 is null (ground level). Also, when an ON signal is not applied to the third signal line 103 while an ON signal is being applied between the first signal line 105 and the second signal line 108, the liquid-crystal potential (V_{LC}) 114 is null (ground level). In this way, the liquid-crystal potential (V_{LC}) 114 is varied, depending on the voltage applied to the third signal line. The potential difference applied to the liquid crystal can be arbitrarily changed by varying the voltage of the signal applied to this signal line.

An offset voltage V_{OFFSET} is applied to a counter electrode 116. The voltage actually applied to the liquid crystal 115 is $V_{GG}+V_{OFFSET}-V_{th}$ or V_{OFFSET}.

In the devices shown in FIGS. 1, 2, and 3, the signal line 8 of the p-channel TFT for one pixel is adjacent to the signal line 6 of the n-channel TFT for the adjacent pixel. When an input signal V_{DD} or V_{SS} is applied, the maximum value of the voltage applied between the signal lines 6 and 8 is $2V_{DD}$ or $2V_{SS}$. However, in the devices shown in FIGS. 16, 17, and 19, the adjacent signal lines 106 and 108 are connected either to the p-channel TFTs or to the n-channel TFTs. In this case, the maximum value of the voltage applied between the signal lines 108 and 106 is only V_{DD} or V_{SS}. Therefore, the amount of leakage between the signal lines 108 and 106 is small.

For example, in the case where an ON signal is applied between the first signal line 105 and the second signal line 108 and an OFF signal is applied between the signal line 106 and the signal line 107 for the duration of the ON signal, only a potential difference of V_{SS} or V_{DD} is applied between the signal lines 108 and 106. This potential difference is half the potential difference applied in the cases of FIGS. 1 to 3. Hence, the amount of leakage between these signal lines is reduced. The spacing between the signal lines can be halved if the same amount of leakage is tolerated.

In the example of FIG. 17, an n-channel TFT 113 and a p-channel TFT 122 form a first complementary TFT pair. An n-channel TFT 124 and a p-channel TFT 125 form a second complementary TFT pair. All of the four gate electrodes of these four TFTs are connected to the third signal line 103. The n-channel TFTs 113 and 124 have a common input terminal which is connected to the second signal line 108 extending in the X-direction. The p-channel TFTs 122 and 125 have a common input terminal connected with a first signal line 105 extending in the X-direction. These two complementary TFT pairs have a common output terminal connected with a pixel electrode 117 which is located on one side of a liquid crystal 115 of a pixel 123. If a slight leakage occurs from one of the two complementary TFT pairs, the pixel electrode can be activated, because they are in phase.

In the example of FIG. 19, two pixel electrodes 117 and 126 and two corresponding complementary TFT pairs are provided for one pixel 123. The two complementary TFT pairs have a common gate electrode to which a first input signal is applied. The input terminals of the two complementary TFT pairs are connected with the first signal line 105 or with the second signal line 108. If one of two TFT pairs for one pixel does not operate due to a trouble such as a leakage from any TFT, the other does operate. If the operation of one pair is delayed, the other operates normally and, therefore, the defective location is not noticeable during the operation of the matrix structure.

In a liquid crystal electro-optical device to which the present invention is applicable, two or more complementary TFT pairs can be provided for one pixel. Furthermore, one pixel may be divided into two or more parts. One or more complementary TFT pairs may be connected to each part.

Dispersion liquid crystal materials used in the present invention comprise transparent substances in solid phase, such as transparent polymers in solid phase and monomers forming high molecules, and nematic, cholesteric, or smectic liquid crystals dispersed in the transparent substances in a granule or spongy state. Examples of the transparent polymers in solid phase include polyethylene, polymethacrylic acid ester, polystyrene, polyvinyl chloride, polyacrylonitrile, polyvinyl alcohol, polyester, polyamide resin, polyethylene terephthalate resin, fluorocarbon resins, and silicone resins. These are used alone or in combination.

A dispersion liquid crystal is prepared by dissolving in a solvent either a mixture of a monomer forming a high molecule and a liquid crystal material or a mixture of a polymer in solid phase as mentioned above and a liquid crystal material. Where the former mixture is employed, it is applied to a substrate and then it is heated or exposed to light to form an electro-optical modulating layer. Where the latter mixture is used, it is dissolved in the solvent, thus producing a liquid. This liquid is applied to a substrate to form a liquid medium layer. Subsequently, this solvent is removed. As a result, a dispersion liquid crystal is obtained.

Examples of the usable solvent include ketones, alcohols, benzene, toluene, and other unsaturated hydrocarbons, and water. One or more solvents are selected appropriately according to the application method. One solvent can be used alone. Also, a mixture of plural solvents can be used. The used method of application is selected according to the shape and the characteristics of the liquid crystal material. A doctor knife, a roll coater, a curtain coater, a knife coater, spraying, spin coating, screen printing, offset printing, and other means can be adopted.

EXAMPLE 1

A liquid crystal display of the circuit configuration of FIG. 1 was used. The arrangement of electrodes and other components corresponding to this circuit configuration is shown in FIG. 6. To simplify the illustration, only the portion which corresponds to a matrix portion of 2×2 is shown. The waveforms of the signals actually used to activate the device are shown in FIG. 10. To simplify the illustration again, signal waveforms used to drive a matrix of 4×4 are next described.

The manner in which the liquid crystal display was fabricated is now described by referring to FIGS. 13(A) to 13(F). In FIG. 13(A), a plate of inexpensive glass 50 withstanding thermal treatment below 700° C., for example, at about 600° C., was prepared. Silicon oxide was sputtered as a 1000 to 3000 Å thick film on the glass 50 by RF (high frequency) sputtering, using a magnetron. In this way, a blocking layer 51 was formed. The atmosphere consisted of 100% oxygen. The film was formed at a temperature of 15° C. The output of the magnetron was 400 to 800 W. The pressure was 0.5 Pa. A target consisting of quartz or a single crystal of silicon was used. The silicon oxide was sputtered at a rate of 30 to 100 Å/min.

A film of silicon was formed on this blocking layer 51 by low-pressure chemical vapor deposition (LPCVD), sputtering, or plasma CVD. Where the film was formed by low-pressure chemical vapor deposition, disilane (Si_2H_6) or trisilane (Si_3H_8) was supplied to a CVD apparatus at a temperature lower than the crystallization temperature by

100° to 200° C., i.e., at 450° to 550° C., for example, 530° C., to create the film. The pressure inside the reaction furnace was 30 to 300 Pa. The film was formed at a rate of 50 to 250 Å/min. In order to make the threshold voltage (V_{th}) for n-channel TFTs substantially equal to the threshold voltage (V_{th}) for p-channel TFTs, boron in the form of diborane could be introduced into the film at 1×10^{15} to 1×10^{18} cm^{-3} during the film formation.

Where sputtering was used, the back pressure prior to the sputtering was 1×10^{-5} Pa or less. A single crystal of silicon was used as a target. The process was carried out within an atmosphere of argon to which 20 to 80% hydrogen was added. For instance, argon and hydrogen accounted for 20% and 80%, respectively. The film was formed at a temperature of 150° C. The frequency was 13.56 MHz. The sputtering output was 400 to 800 W. The pressure was 0.5 Pa.

Where a silicon film was formed by plasma CVD, silane (SiH_4) or disilane (Si_2H_6) was used at a temperature of, for example, 300° C. The material was admitted into a PCVD apparatus and the film was formed by applying an RF power of 13.56 MHz.

The film formed by these methods preferably contains oxygen atoms of 5×10^{21} atoms·cm^{-3}. If this oxygen concentration is high, crystallization does not easily take place. Therefore, the annealing temperature or the annealing time must be increased. If the oxygen concentration is too low, then the leakage current in OFF state will be increased by backlighting. For these reasons, the preferable range is between 4×10^{19} and 4×10^{21} atoms·cm^{-3}. The hydrogen concentration is for example 4×10^{20} atoms·cm^{-3}. Compared with the amount of the silicon concentration of 4×10^{22} atoms·cm^{-3} the hydrogen is 1 atomic % In order to promote the crystallization at the sources and drains, the oxygen concentration is 7×10^{19} atoms·cm^{-3} or less, preferably 1×10^{19} atoms·cm^{-3} or less. Ions of oxygen may be implanted only into the regions which become channels of TFTs forming pixels at 5×10^{20} to 5×10^{21} atoms·cm^{-3}. At this time those TFTs which form peripheral circuits are not illuminated with light. Therefore, reducing the oxygen concentration for obtaining a larger carrier mobility is effective in permitting operation at high frequencies.

After an amorphous silicon film 500 to 5000 Å thick, e.g., 1500 Å, was formed, it was heated at a moderate temperature of 450° to 700° C. for 12 to 70 hours within a non-oxidizing atmosphere. For example, it was allowed to stand at 600° C. within an atmosphere of hydrogen. Since the amorphous silicon oxide film was formed on the surface of the substrate and under the silicon film, no specific nuclei existed during the thermal treatment; rather the whole laminate was uniformly annealed. That is, when the film was created, it had an amorphous structure. The hydrogen was merely added to it.

The silicon film is changed from the amorphous structure to a highly oriented state by the annealing. Some of the film assumes a crystalline state. Especially, after the silicon film is formed, the relatively highly oriented zones tend to crystallize. However, these zones are bonded to each other by the intervening silicon atoms. Therefore, the silicon atoms attract each other. A peak shifted from a single crystal silicon peak of 522 cm^{-1} toward lower frequencies is observed by laser Raman spectroscopy. When calculated from the half-value width, the apparent particle diameter is 50 to 500 Å, which means a microcrystal. In practice, however, there are numerous highly crystalline zones which form clusters. In this way, a semi-amorphous film can be formed in which the clusters are anchored to each other by silicon atoms.

Consequently, the film is substantially free of grain boundaries. Because carriers can easily move from cluster to cluster through the anchored locations, the carrier mobility is higher than the carrier mobility in polycrystalline silicon where clear grain boundaries exist. That is, the hole mobility (μh)= 10 to 200 $cm^2/V\cdot s$. The electron mobility (μe)=15 to 300 $cm^2/V\cdot s$.

On the other hand, where the film is made polycrystalline by annealing at a high temperature of 900° to 1200° C. not at a moderate temperature as described above, impurities segregate by solid-phase growth from nuclei, so that impurities such as oxygen, carbon, and nitrogen are collected in quantity at the grain boundaries. Although the mobility in the crystal is large, barriers are created at the grain boundaries. Thus, movement of carries is hindered. The actual situation is that it is difficult to obtain mobilities greater than 10 $cm^2/V\cdot s$. In the present example, semi-amorphous or semi-crystal semiconductors are used for these reasons.

In FIG. **13**(A), a silicon film was etched photolithographically, using a first photomask (1). A region **22** having a channel width of 20 μm and becoming a p-channel TFT was formed to the right in the figure. A region **13** becoming an n-channel TFT was formed to the left.

A silicon oxide film was formed on this silicon film as a gate-insulating film having a thickness of 500 to 2000 Å, e.g., 1000 Å. This silicon oxide film was created under the same conditions as in the process for fabricating the silicon oxide film acting as the blocking layer. A small amount of fluorine could be doped into the silicon oxide film to fix sodium ions.

Thereafter, a silicon film or a multilayer film including this silicon film was formed on the silicon oxide film. The silicon film was doped with phosphorus at 1 to 5×10^{21} atoms·cm^{-3}. The multilayer film comprised the silicon film and an overlying film of molybdenum, tungsten, $MoSi_2$, or WSi_2. This silicon or multilayer film was patterned, using a second photomask (2). As a result, a laminate shown in FIG. **13**(B) was derived. Gate electrodes **55** and **56** for p-channel and n-channel TFTs, respectively, were formed. For example, the channel length was 10 μm. To form the gate electrodes, phosphorus-doped silicon was deposited to a thickness of 0.2 μm and then molybdenum was deposited on it to a thickness of 0.3 μm. In FIG. **13**(C), a photoresist **57** was formed, using a photomask (3). Ions of boron were implanted into the source **59** and the drain **58** of the p-channel TFT at a dose of 1 to 5×10^{15} cm^{-2}. As shown in FIG. **13**(D), a photoresist **61** was formed, using a photomask (4). Ions of phosphorous were lodged into the source **64** and the drain **62** of the n-channel TFT at a dose of 1 to 5×10^{15} cm^{-2}.

These ions were implanted through a gate-insulating film **54**. In FIG. **13**(B), it is also possible that the silicon oxide on the silicon film is removed, using the gate electrodes **55** and **56** as masks and then ions of boron and phosphorus are implanted directly into the silicon film.

Then, annealing was again effected at 600° C. for 10 to 50 hours. The dopant in the source **59** and drain **58** of the p-channel TFT was activated so that the TFT may be doped p^+-type. Also, the dopant in the source **64** and drain **62** of the n-channel TFT was activated so that the TFT may be doped n^+-type. Regions **60** and **63** forming channels were formed as semi-amorphous semiconductors under the gate electrodes **55** and **56**.

Thus, complementary TFTs could be fabricated without elevating the temperature above 700° C. in any step, though self-aligned ion implantation was utilized. Therefore, it is

not necessary to fabricate the substrates from an expensive material such as quartz. In this way, this process is quite suitable for fabrication of a liquid crystal display having a large number of pixels.

In the present example, the annealing step was carried out twice as shown in FIGS. **13**(A) and **13**(D). Depending on the desired characteristics, the annealing step of FIG. **13**(A) can be omitted. In this case, the two annealing steps are carried out simultaneously in the step of FIG. **13**(D). As a result, the manufacturing time is shortened. In FIG. **13**(E), an interlayer insulator **65** was sputtered to form a silicon oxide film. This film can be created by LPCVD, photo-assisted CVD, or atmospheric pressure CVD. For example, the thickness is 0.2 to 0.6 μm. Then, windows (openings) **66** for electrodes were formed, using a photomask (5). Aluminum was sputtered on the whole laminate. Leads **71**, **72** and contacts **67**, **68** were fabricated, using a photomask (6). Subsequently, a planarizing organic resin **69**, such as transparent polyimide resin, was applied to the surface. Again, holes (openings) were formed for electrodes, using a photomask (7).

As shown in FIG. 13(F), a complementary structure was built from two TFTs. The output terminal of this complementary structure was connected with one transparent electrode for one pixel of a liquid-crystal. For this purpose, a film of indium tin oxide (ITO) was formed by sputtering. This film was etched, using a photomask (8) to form an electrode **70**. This ITO film was created at a temperature between room temperature and 150°C. and annealed at 200° C. to 400° C. within an atmosphere of oxygen or air. In this way, the p-channel TFT **22**, the n-channel TFT **13**, and the electrode **70** consisting of a transparent conductive film were created on the same glass substrate **50**. The electrical characteristics of the obtained TFTs were as follows. The mobility in the p-channel TFT was 20 $cm^2/V \cdot s$ and the threshold value V_{th} was −5.9 V. The mobility in the n-channel TFT was 40 $cm^2/V \cdot s$, and the threshold voltage V_{th} was 5.0 V.

A uniform solution was prepared from denatured acrylic resin (such as manufactured by World Rock Co., Ltd, under the product name 880K1) which hardens when exposed to light and from a nematic liquid crystal (E44). The solution was applied to one substrate that was fabricated as described above for use in a liquid crystal display, by screen printing to a thickness of 10 μm. This substrate and another substrate having transparent electrodes over the whole surface were bonded together at a reduced pressure. A pressure of 2 kg/cm^2 was applied from above. At the same time, ultraviolet radiation was directed to the device from below to form a liquid crystal cell. The arrangement of the electrodes of this liquid crystal display is shown in FIG. **6**. The n-channel TFT **13** was formed at the intersection of a first scanning line **5** and a data line **3**. An n-channel TFT for other pixel was similarly formed at the intersection of the first scanning line **5** and a data line **4**. Meanwhile, the p-channel TFT was formed at the intersection of a second scanning line **8** and the data line **3**. An n-channel TFT for other pixel was formed at the intersection of another adjacent first scanning line **6** and the data line **3**. In this way, a matrix structure using complementary TFT pairs was created. The n-channel TFT **13** was connected with the first scanning line **5** via the contact at the input terminal of a drain **10**. A gate **9** was connected with the data line **3** in which multilayered interconnects were formed. The output terminal of a source **12** was connected with the pixel electrode **17** via a contact.

Meanwhile, with respect to the p-channel TFT **22**, the input terminal of the drain **20** was connected to the second scanning line **8** via a contact. Its gate **21** was connected with the data line **3**. The output terminal of the source **18** was connected with the pixel electrode **17** via a contact, in the same way as the n-channel TFT. In this way, one pixel **23** was constituted by the transparent pixel electrode **17** and the complementary TFTs between the scanning lines **5** and **8**. This structure can be repeated horizontally and vertically to extend the matrix of 2×2 to a larger matrix of 640×480 or 1280×960. In this manner, a liquid crystal display having a large area can be manufactured.

This structure is characterized in that the pixel electrode **17** is locked at any one of three values of the liquid-crystal potential V_{LC} because a pair of complementary TFTs is provided for one pixel. The operation is next described by referring to FIGS. **9** and **10**. FIG. **9** is a circuit diagram of a liquid crystal display having pixels arranged in 4 rows and 4 columns. FIG. **10** is a timing chart showing the waveforms of signals activating the display.

In the present example, each of pairs X_{1a} and X_{1b}, X_{2a} and X_{2b}, X_{3a} and X_{3b}, and X_{4a} and X_{4b} acts as a pair of scanning lines. Y_1, Y_2, Y_3, and Y_4 serve as data lines. In FIG. **9**, AA, AB, . . . , DD mean the addresses of pixels at the corresponding locations.

This liquid crystal display has pixels of a matrix of 4×4. FIG. **10** is a timing chart showing the waveforms of signals applied to the four pixels at the four addresses AA, AB, BA, and BB, the liquid-crystal potential, and the potential difference actually applied to the liquid crystal. In FIG. **10**, the horizontal axis indicates time. It is assumed that one frame begins at instant of time T_1 and ends at instant of time T_2. This frame is divided into four. Four scanning line pairs are successively scanned to apply a scanning signal. In the figure, only X_{1a}, X_{2a}, X_{3a}, and X_{4a} are shown. In practice, however, signals which are identical in waveshape with the signals applied to X_{1a}, X_{2a}, X_{3a}, and X_{4a} but differ in polarity from these signals are applied to lines X_{1b}, X_{2b}, X_{3b}, and X_{4b}. Data signals as shown in FIG. **10** are applied to lines Y_1, Y_2, Y_3 and Y_4. During the period between instants T_1 and T_2, only pixel at the address AA is selected and activated or deactivated. In particular, a data signal is applied to the data line Y_1 during the period between instants T_1 and t_1. A voltage exceeding the threshold value is applied to the liquid crystal at the pixel at the address AA during this period to activate the liquid crystal. At this time, an offset voltage is applied to the counter electrode of the liquid crystal display. In FIG. **10**, exactly the same signal waveform is applied during the next period between instants T_2 and T_3 to activate the liquid crystal at the address AA.

During the period between instants T_3 and T_4 and during the period between instants T_4 and T_5, a signal is applied to select none of the four pixels. During the period between instants T_5 and T_6, a signal for selecting the pixel at the address AA again is applied.

During the period between instants T_6 and T_8, the signals applied to the data lines are inverted. An offset voltage which differs in polarity from the signal applied during the period between instants T_1 and T_6 is applied to the counter electrode. An AC signal is applied to the liquid crystal. The electric charge which was displaced in the positive direction during the period between instants T_1 and T_6 can be eliminated by this AC signal. Specifically, of the signal applied during the period between instants T_2 and T_4, the signals applied to the lines Y_1, Y_2, Y_3, and Y_4 are inverted, i.e., the select signals and non-select signals are interchanged. The polarity of the offset voltage applied to the counter electrode is inverted. In the first half, or one frame, of the period between the instants T_2 and T_4, the AC signal is applied and the liquid crystal is so activated that the pixel at the address

AA is selected, while in the second half, or one frame, of the period, none of the four pixels are selected. In this way, the electric charge remaining on the pixels can be removed.

As described above, the potential difference actually applied to the liquid crystal is the difference between the voltage applied to the third signal line, in the present example the pulse voltage applied to the data lines plus the offset voltage applied to the counter electrode, and the threshold voltage V_{th} for the TFTs. Therefore, the potential difference actually applied to the liquid crystal can be controlled by controlling the pulse voltage. This permits display to be provided at various gray levels. This activation method is especially suitable for liquid crystals having no distinct threshold values, e.g., dispersion liquid crystals having smooth threshold values, and satisfactory gradation display can be provided.

In this way, in the novel activation method, the liquid crystal can be made to provide display simply by applying very simple pulse signals to the data lines and the scanning line pairs.

Another gradation display method is to apply activating signals for plural frames to one display screen. Where one screen is displayed, the number of the select signals applied to each one pixel can be made less than the total number of the frames. This facilitates gradation display.

No polarizing sheets are necessary in case of the dispersion liquid crystal display. In order to increase the switching speed of the liquid crystal, the operation voltage is set to ±10 to ± 15 V. The spacing of the cell is set to about 1 to 20 μm.

Since the novel liquid crystal display using a dispersion liquid crystal needs no polarizing sheets, the quantity of light can be increased, whether the display is of the reflection type or of the transmission type. Furthermore, this liquid crystal has no threshold values. In the present invention, the complementary TFTs have clear threshold voltages. Therefore, a large contrast can be obtained. Also, crosstalk between successive pixels can be eliminated.

In the present example, the TFTs can be fabricated from materials other than the materials described above.

EXAMPLE 2

This example is executed, using the structure of the liquid crystal display shown in FIGS. **2** and **7**. As can be seen from these figures, a scanning line **3** extending in the Y-direction is disposed in the center. One pixel **23** is formed between a first data line **5** and a second data line **8** of a pair of data lines. One pixel comprises a pixel electrode **17** made from a transparent conductive film and two complementary TFT pairs connected to the pixel electrode **17** and comprising two n-channel TFTs **13** and **24** and two p-channel TFTs **22** and **25**. All the gate electrodes are connected to the scanning line **3**. The two n-channel TFTs are connected with the first data line **5**. The two p-channel TFTs are connected to the second data line **8**. If any one of the two complementary TFT pairs malfunctions because of a leakage between the gate electrode and the channel formation region, the pixel functions normally.

This structure is characterized in that the pixel electrode **17** is locked at any one of three values of the liquid-crystal potential V_{LC} because two complementary TFT pairs are provided for one pixel. The operation is next described by referring to FIGS. **9** and **11**. FIG. **9** is a circuit diagram of a liquid crystal display having a matrix structure of 4×4. FIG. **11** is a timing chart of the waveforms of signals activating the display.

In the present example, each of pairs X_{1a} and X_{1b}, X_{2a} and X_{2b}, X_{3a} and X_{3b}, and X_{4a} and X_{4b} acts as a pair of data lines. Y_1, Y_2, Y_3 and Y_4 serve as scanning lines. In FIG. **9**, AA, AB, . . . , DD mean the addresses of pixels at the corresponding locations.

This liquid crystal display has pixels of a matrix of 4×4. FIG. **11** is a timing chart showing the waveforms of signals applied to the four pixels at the four addresses AA, AB, BA, and BB, the liquid-crystal potential, and the potential difference actually applied to the liquid crystal. In FIG. **11**, the horizontal axis indicates time. It is assumed that one frame begins at instant T_1 and ends at instant T_2. This frame is divided into four. Scanning lines Y_1, Y_2, Y_3, and Y_4 are successively scanned to apply a scanning signal. Data signals as shown in FIG. **11** are applied to X_1, X_2, X_3, and X_4 lines. In the figure, only X_{1a}, X_{2a}, X_{3a}, and X_{4a} are shown. In practice, however, signals which are identical in waveshape with the signals applied to X_{1a}, X_{2a}, X_{3a}, and X_{4a} but differ in polarity from these signals are applied to lines X_{1b}, X_{2b}, X_{3b}, and X_{4b}. During the period between instants T_1 and T_2, only pixel at the address AA is selected and activated or deactivated. In particular, a data signal is applied to the data line X_1 during the period between instants T_1 and t_1. A voltage exceeding the threshold value is applied to the liquid crystal at the pixel at the address AA during this period to activate the liquid crystal. At this time, an offset voltage (electric potential) is applied to the counter electrode of the liquid crystal display. In FIG. **11**, exactly the same signal waveform is applied during the next period between instants T_2 and T_3 to activate the liquid crystal at the address AA.

During the period between instants T_3 and T_4 and during the period between instants T_4 and T_5, a signal is applied to select none of the four pixels. During the period between instants T_5 and T_6, a signal for selecting the pixel at the address AA again is applied.

During the period between instants T_6 and T_8, the signals applied to the data lines are inverted. An offset voltage (electric potential) which differs in polarity from the signal applied during the period between instants T_1 and T_6 is applied to the counter electrode. An AC signal is applied to the liquid crystal. The electric charge which was displaced in the positive direction during the period between instants T_1 and T_6 can be eliminated by this AC signal. Specifically, of the signal applied during the period between instants T_2 and T_4, the signals applied to the lines X_1, X_2, X_3, and X_4 are inverted, i.e., the select signals and non-select signals are interchanged. The polarity of the offset voltage applied to the counter electrode is inverted. In the first half, or one frame, of the period between the time T_2 and the time T_4, the AC signal is applied and the liquid crystal is so activated that the pixel at the address AA is selected, while in the second half, or one frame, of the period, none of the four pixels are selected. In this way, the liquid crystal is activated.

In this manner, in the novel activation method, the liquid crystal can be made to provide display simply by applying very simple pulse signals to the data lines and the scanning line pairs. Also, gradation display can be provided by varying the signal voltages applied to the scanning lines, in the same way as in Example 1.

EXAMPLE 3

This example is executed, using the structure of the liquid crystal display shown in FIGS. **3** and **8**. As can be seen from these figures, a data line **3** extending in the Y-direction is disposed in the center. One pixel **23** is formed between a first

scanning line **5** and a second scanning line **8** of a pair of scanning lines. One pixel comprises two pixel electrodes **17** and **26** consisting of a transparent conductive film. A complementary TFT pair consisting of an n-channel TFT **13** and a p-channel TFT **22** is connected with the pixel electrode **17**. A complementary TFT pair consisting of an n-channel TFT **24** and a p-channel TFT **25** is connected with the pixel electrode **26**. All the gate electrodes are connected to the data line **3**. The two n-channel TFTs are connected with the first scanning line **5**. The two p-channel TFTs are connected to the second scanning line **8**. If any one of the two complementary TFT pairs malfunctions because of a leakage between the gate electrode and the channel formation region, the pixel functions normally. Therefore, if one pixel electrode should fail to operate satisfactorily, the other pixel electrode operates normally. Where the device is a color liquid crystal display, deterioration in the gray scale can be alleviated.

The operation is next described by referring to FIGS. **9** and **12**. FIG. **9** is a circuit diagram of a liquid crystal display having a matrix structure of 4×4. FIG. **12** is a timing chart of the waveforms of signals activating the display.

In the present example, each of pairs X_{1a} and X_{1b}, X_{2a} and X_{2b}, X_{3a} and X_{3b}, and X_{4a} and X_{4b} acts as a pair of scanning signal lines. Y_1, Y_2, Y_3, and Y_4 serve as data lines. In FIG. **9**, AA, AB, . . . , DD mean the addresses of pixels at the corresponding locations.

This liquid crystal display has pixels of a matrix of 4×4. FIG. **12** is a timing chart showing the waveforms of signals applied to the four pixels at the four addresses AA, AB, BA, and BB, the liquid-crystal potential, and the potential difference actually applied to the liquid crystal. In FIG. **12**, the horizontal axis indicates time. It is assumed that one frame begins at instant T_1 and ends at instant T_2. This frame is divided into 16. The four scanning line pairs are successively scanned to apply a scanning signal. Although only lines X_{1a}, X_{2a}, X_{3a}, and X_{4a} are shown in the figure, signals which are identical in waveform with the signals applied to the lines X_{1a}, X_{2a}, X_{3a}, and X_{4a} but differ in polarity from these signals are applied to the lines X_{1b}, X_{2b}, X_{3b}, and X_{4b}. Data signals as shown in FIG. **12** are applied to lines Y_1, Y_2, Y_3, and Y_4. The timing is determined by the addresses of the selected pixels. A data signal is applied to the data lines during a certain one of the 16 periods within one frame. The duration of the signal applied to the line Y_1, Y_2, Y_3, or Y_4 is one-fourth as long as that of the signal applied to X_{1a}, X_{1b}, X_{2a}, X_{2b}, X_{3a}, X_{3b}, X_{4a}, or X_{4b}. During the period between instants T_1 and T_2, only the pixel at the address AA is selected and activated or deactivated. In particular, a data signal is applied to the data line Y_1 during the period between instants T_1 and t_1. A voltage exceeding the threshold value is applied to the liquid crystal at the pixel at the address AA during this period to activate the liquid crystal. At this time, an offset voltage is applied to the counter electrode of the liquid crystal display. During the succeeding period between instants T_2 and T_3, a signal is applied to select none of the four pixels.

During the period between instants T_3 and T_4, the signals applied to the data lines are inverted. An offset voltage which differs in polarity from the signal applied during the period between instants T_1 and T_3 is applied to the counter electrode. An AC signal is applied to the liquid crystal. The electric charge which was displaced in the positive direction during the period between instants T_1 and T_3 can be eliminated by this AC signal. Specifically, of the signals applied during the period between instants T_1 and T_2, the signals applied to the lines Y_1, Y_2, Y_3, and Y_4 are inverted, i.e., the select signals and non-select signals are interchanged. The polarity of the offset voltage applied to the counter electrode is inverted. In the first half of the frame, the AC signal is applied and the liquid crystal is so activated that the pixel at the address AA is selected, while in the second half of the frame, none of the four pixels are selected.

In this way, in the novel activation method, the liquid crystal can be made to provide display simply by applying very simple pulse signals to the data lines and the scanning line pairs. In the present example, the Y lines are taken as the scanning lines. The invention is not limited to this scheme. It is also possible that the X lines are taken as the scanning lines. Furthermore, data signals may be applied to the data lines at random, and pixels may be selected at random. This example is similar to Examples 1 and 2 in other respects.

EXAMPLE 4

A liquid crystal display of the circuit configuration of FIG. **16** was used. The arrangement of electrodes and other components corresponding to this circuit configuration is shown in FIG. **20**. To simplify the illustration, only the portion which corresponds to a matrix portion of 2×2 is shown.

Circuits, electrodes, etc. (FIGS. **16** and **20**) on a first substrate were fabricated in the same way as in Example 1. A second substrate having transparent electrodes over the whole surface was bonded to the first substrate to form a liquid crystal cell. A twisted nematic liquid crystal material was injected into the cell. The arrangement of the electrodes of this liquid crystal display is shown in FIG. **20**. An n-channel TFT **113** was formed at the intersection of a first scanning line **105** and a third signal line **103**. An n-channel TFT for other pixel was similarly formed at the intersection of the first scanning line **105** and another third signal line **104**. A p-channel TFT was formed at the intersection of the second signal line **108** and the third signal line **103**. A p-channel TFT for other pixel was formed at the intersection of an adjacent first scanning line **106** and the third signal line **103**. Similarly, a p-channel TFT was formed at the intersection of the first signal line **106** and the third signal line **104**. In this way, a matrix structure using complementary TFT pairs was created. The n-channel TFT **113** was connected with the first scanning line **105** via the contact at the input terminal of a drain **110**. A gate **109** was connected with the signal line **103** in which multilayered interconnects were formed. The output terminal of a source **112** was connected with a pixel electrode **117** via a contact.

Meanwhile, with respect to a p-channel TFT **122**, the input terminal of the drain **120** was connected to the second scanning line **108** via a contact. Its gate **121** was connected with the signal line **103**. The output terminal of the source **118** was connected with the pixel electrode **117** via a contact, in the same way as in the case of the n-channel TFT. With respect to the adjacent complementary TFT pair connected with the same third signal line, the p-channel TFT **522** is connected with the second signal line **106**, while the n-channel TFT **513** is connected with the first signal line **107**. The second signal lines which were connected to the p-channel TFTs were adjacent to each other. In this way, one pixel **123** was formed by a pixel electrode **117** and the complementary TFTs between the signal lines **105** and **108**. The pixel electrode **117** consisted of a transparent conductive film. This structure can be repeated horizontally and vertically to extend the matrix of 2×2 to a larger matrix of 640×480 or 1280×960. In this manner, a liquid crystal display having a large number of pixels can be manufactured.

This structure is characterized in that the pixel electrode **117** is locked at any one of three values of the liquid-crystal potential V_{LC} because two complementary TFT pairs are provided for one pixel. Furthermore, only a small amount of leakage occurs, because the p-channel TFTs are adjacent to each other, and because the maximum value of the potential difference applied between the signal lines connected to these p-channel TFTs is only V_{SS}.

As described above, the potential difference actually applied to the liquid crystal is the difference between the voltage applied to the third signal line, in the present example the pulse voltage applied to the data lines plus the offset voltage applied to the counter electrode, and the threshold voltage V_{th} for the TFTs. That is, if the pulse voltage applied to the signal lines is varied, the potential difference actually applied to the liquid crystal varies accordingly. This permits display to be provided at various gray levels. This activation method is especially suitable for liquid crystals having no distinct threshold values, e.g., dispersion liquid crystals having smooth threshold values, and satisfactory gradation display can be provided.

Another gradation display method is to apply activating signals for plural frames to one display screen. Where one screen is displayed, the number of the select signals applied to each one pixel can be made less than the total number of the frames. This facilitates gradation display.

In the present example, where a twisted nematic liquid crystal material is used, the spacing between the substrates is about 10 μm. Orientation films are formed on both transparent conductive films. The orientation films are required to be rubbed.

Where a ferroelectric liquid crystal material is employed, the operation voltage is set to ±20 V. The spacing of the cell is set to 1.5 to 3.5 μm, for example, 2.3 μm. An orientation film is formed only on the counter electrode **116** and rubbed.

Where a dispersion liquid crystal or polymeric liquid crystal is used, no orientation film is needed. To increase the switching speed, the operation voltage is set to ±10 to ±15 V. The spacing of the cell is set to only 1 to 10 μm.

Especially, where a dispersion liquid crystal is used, no polarizing sheets are needed, so the quantity of light can be increased, whether the display is of the reflection type or of the transmission type. Furthermore, this liquid crystal has no threshold values. In the present invention, the complementary TFTs have clear threshold voltages. Therefore, a large contrast can be obtained. Also, crosstalk between successive pixels can be eliminated.

EXAMPLE 5

This example is executed, using the structure of the liquid crystal display shown in FIGS. **17** and **21**. As can be seen from these figures, a signal line **103** extending in the Y-direction is disposed in the center. One pixel **123** is formed between a first signal line **105** and a second signal line **108** of a pair of signal lines. One pixel is connected with a pixel electrode **117** consisting of a transparent conductive film and with two complementary TFT pairs comprising two n-channel TFTs **113** and **124** and two p-channel TFTs **122** and **125**. All the gate electrodes are connected to the third signal line **103**. The two n-channel TFTs are connected with the second signal line **108**. The two p-channel TFTs are connected to the first signal line **105**. n-channel TFTs of complementary TFT pairs for an adjacent pixel are connected with the second signal line **106**, while p-channel TFTs are connected with the first signal line **107**. If any one of the two complementary TFT pairs of one pixel malfunctions because of a leakage between the gate electrode and the channel formation region, the pixel functions normally.

This structure is characterized in that the pixel electrode **117** is locked at any one of three values of the liquid-crystal potential V_{LC} because two complementary TFT pairs are provided for one pixel. Furthermore, only a small amount of leakage occurs, because the n-channel TFTs of adjacent pixels are adjacent to each other, and because the maximum value of the potential difference applied between the signal lines connected to these n-channel TFTs is only V_{SS}.

A method of activating this structure is now described by referring to FIG. **18**. As shown in this figure, when an ON signal is applied to the third signal line **103** while an ON signal is being applied to the first signal line **105** and to the second signal line **108**, the liquid-crystal potential (V_{LC}) **114** is equal to the voltage V_{DD} applied to the first signal line. When an OFF signal is applied to the third signal line **103** while an OFF signal is being applied between the first signal line **105** and the second signal line **108** which form a pair, the liquid-crystal potential (V_{LC}) **114** is null (ground level). When an ON signal is not applied to the third signal line **103** while an OFF signal is being applied between the first signal line **105** and the second signal line **108** forming a pair, the liquid-crystal potential (V_{LC}) **114** is equal to the voltage V_{SS} applied to the second signal line. Thus, the liquid-crystal potential (V_{LC}) **114** is locked either at V_{DD} or at V_{SS}. Hence, floating condition does not take place.

EXAMPLE 6

This example is executed, using the structure of the liquid crystal display shown in FIGS. **19** and **22**. As can be seen from these figures, a signal line **103** extending in the Y-direction is disposed in the center. One pixel **123** is formed between a first signal line **105** and a second signal line **108** of a pair of signal lines, and comprises two pixel electrodes **117** and **126** consisting of a transparent conductive film. A complementary TFT pair consisting of an n-channel TFT **113** and a p-channel TFT **122** is connected with the pixel electrode **117**. A complementary TFT pair consisting of an n-channel TFT **124** and a p-channel TFT **125** is connected with the pixel electrode **126**. All the gate electrodes are connected to the signal line **103**. The two n-channel TFTs are connected with the first scanning line **105**. The two p-channel TFTs are connected to the second signal line **108**. With respect to the complementary TFTs provided for an adjacent pixel, the p-channel TFTs are connected to the second signal line **106**, while the n-channel TFTs are connected to the first signal line **107**. If any one of the two complementary TFT pairs malfunctions because of a leakage between the gate electrode and the channel formation region, the pixel functions normally. Therefore, if one pixel electrode should fail to operate satisfactorily, the other pixel electrode operates normally. Where the device is a color liquid crystal display, deterioration in the gray scale can be alleviated.

In the present example, the two second signal lines **108** and **106** which are formed between adjacent pixels are made of the same material. First, this material is deposited on a substrate. Then, the material is patterned to form one interconnect. Subsequently, this interconnect is divided into two by irradiation of an excimer laser beam. As a result, the two signal lines are formed. In this case, the spacing between the two signal lines can be made small. Also, the numerical aperture ratio of the display device can be improved. Fur-

thermore, accuracy required for the mask used in the manufacturing process is not very strict. Consequently, the production yield can be enhanced. Further, the costs of the mask can be reduced.

As described thus far, in the novel activation method, the liquid crystal is not at floating potential and so stable display can be provided. Also, the complementary TFTs acting as active devices are excellent in ability to activate liquid crystal. This allows the operation margin to be extended. In addition, the peripheral driving circuits can be made simpler. This is effective in reducing the size of the display device and the manufacturing cost. Moreover, the liquid crystal can be activated very well merely by applying very simple signals to the three signal lines and to the counter electrode. If any one of the TFTs is defective, it can be compensated for to some extent, because the outputs are in phase. Further, no leakage occurs, because a high potential difference is not applied between the signal lines connected to adjacent pixel electrodes. Additionally, the numerical aperture ratio of the display device can be enhanced, since the adjacent signal lines can be spaced close to each other.

A transmission liquid crystal display or reflection liquid crystal display can be used as a display medium according to the present invention. Usable liquid crystal materials include the aforementioned twisted nematic liquid crystals, ferroelectric liquid crystals, dispersion liquid crystals, and polymeric liquid crystals (polymer liquid crystals). Also, phase transition liquid crystals can also be utilized. These phase transition liquid crystals are fabricated in the manner described now. Dopant ions are added to nematic liquid crystals of the guest host type or of the anisotropic dielectric type. An electric field is applied to these liquid crystals, thus producing nematic liquid crystals. The obtained nematic liquid crystals are mixed with cholesteric liquid crystals. An electric field is applied to the mixtures, so that a phase transition takes place between the nematic phase and the cholesteric phase. In this way, the display is made either transparent or opaque. With respect to materials other than liquid crystals, media for so-called electrophoretic displays can be used. These media are prepared by dispersing pigment particles in organic solvents colored, for example, with dyestuffs which differ in color from the pigment particles.

In order to prevent the liquid crystal material from being electrolyzed, it is essential that an AC signal is applied. This application of the AC signal is easily achieved by inverting the signal applied to the gate signal lines of the complementary TFTs and inverting the polarity of the offset voltage applied to the counter electrode.

If the voltage of the signal applied to the third signal line is varied at will, then the potential difference actually applied to the liquid crystal is varied accordingly. This permits gradation display. This activation method is especially suited for liquid crystals having mild (smooth) threshold values, for example dispersion liquid crystals. In this case, satisfactory gradation display can be provided. Where signals for driving plural frames are applied to a liquid crystal to display one viewing screen, the number of the select signals applied to each one pixel is made fewer than the total number of the frames. Hence, gradation display can be readily attained.

The foregoing description of preferred embodiments has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form described, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen in order to explain most clearly the principles of the invention and its practical application thereby to enable others in the art to utilize most effectively the invention in various embodiments and with various modifications as are suited to the particular use contemplated.

What is claimed is:

1. An electro-optical device comprising:

a substrate having an insulating surface; and

at least two thin film transistors formed on said substrate,

wherein at least a channel of each of said thin film transistors contains oxygen at 4×10^{19} to 4×10^{21} atoms/cm^3.

2. The device of claim 1 wherein said substrate comprises glass covered with a silicon oxide layer.

3. The device of claim 1 wherein each said thin film transistor has a gate insulating comprising silicon oxide doped with fluorine.

4. The device of claim 1 wherein said channel comprises silicon.

5. The device of claim 4 wherein said silicon is doped with hydrogen.

6. An electro-optical device comprising:

a substrate having an insulating surface; and

at least two thin film transistors formed on said substrate,

wherein a channel of each of said thin film transistors contains oxygen at 5×10^{20} to 5×10^{21} atoms/cm^3 and a source and a drain of each of said thin film transistors contains oxygen at 7×10^{19} atoms/cm^3 or less.

7. The device of claim 6 wherein said substrate comprises glass covered with a silicon oxide layer.

8. The device of claim 6 wherein each said thin film transistor has a gate insulating comprising silicon oxide doped with fluorine.

9. The device of claim 6 wherein said channel comprises silicon.

10. The device of claim 6 wherein said silicon is doped with hydrogen.

11. An electro-optical device comprising:

a substrate having an insulating surface; and

a plurality of pixel electrodes formed on said substrate in a matrix form, each of said pixel electrodes connected with at least one thin film transistor,

wherein a channel of said thin film transistors contains oxygen at 4×10^{19} to 4×10^{21} atoms/cm^3.

12. The device of claim 11 wherein said substrate comprises glass covered with a silicon oxide layer.

13. The device of claim 11 wherein each said thin film transistor has a gate insulating comprising silicon oxide doped with fluorine.

14. The device of claim 11 wherein said channel comprises silicon.

15. The device of claim 14 wherein said silicon is doped with hydrogen.

16. An electro-optical device comprising:

a substrate having an insulating surface; and

a plurality of pixel electrodes formed on said substrate in a matrix form, each of said pixel electrodes connected with at least one thin film transistor,

wherein a channel of said thin film transistors contains oxygen at 5×10^{20} to 5×10^{21} atoms/cm^3 and a source and a drain thereof contains oxygen at 7×10^{19} atoms/cm^3 or less.

17. The device of claim 16 wherein said substrate comprises glass covered with a silicon oxide layer.

18. The device of claim 16 wherein each said thin film transistor has a gate insulating comprising silicon oxide doped with fluorine.

19. The device of claim 16 wherein said channel comprises silicon.

20. The device of claim 19 wherein said silicon is doped with hydrogen.

21. An active matrix display device comprising:

a glass substrate;

a plurality of pixel electrodes formed on said substrate;

a plurality of thin film semiconductor devices formed on said substrate and connected to said pixel electrodes;

a peripheral circuit comprising thin film transistors formed on said substrate,

wherein said thin film transistors of said peripheral circuit include channel semiconductor layers having at least one of an electron mobility of 15–300 $cm^2/V \cdot s$ and a hole mobility of 10–200 $cm^2/V \cdot s$.

22. The device of claim 21 wherein said channel semiconductor layers comprise silicon in which oxygen is contained at a concentration not higher than 7×10^{19} atoms/cm^3.

23. An active matrix display device comprising:

a glass substrate;

a plurality of pixel electrodes formed on said substrate;

a plurality of thin film semiconductor devices formed on said substrate and connected to said pixel electrodes;

a peripheral circuit comprising thin film transistors formed on said substrate,

wherein said thin film transistors of said peripheral circuit have a channel semiconductor layer comprising silicon in which oxygen is contained at a concentration not higher than 7×10^{19} atoms/cm^3.

* * * * *

APPENDIX C

***Chiba* Reference**

U.S. Patent No. 5,589,960

US005589960A

United States Patent [19]

Chiba et al.

[11] Patent Number: 5,589,960

[45] Date of Patent: Dec. 31, 1996

[54] **LIQUID CRYSTAL DISPLAY SYSTEM**

[75] Inventors: **Masao Chiba; Mikio Ishii**, both of Saitama, Japan

[73] Assignee: **Kansei Corporation**, Saitama, Japan

[21] Appl. No.: **359,453**

[22] Filed: **Dec. 20, 1994**

[30] **Foreign Application Priority Data**

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Mar. 1, 1994 [JP] Japan 6-031349

[51] **Int. Cl.**[6] **G02F 1/133**; G02F 1/1335

[52] **U.S. Cl.** **349/76**; 349/72; 349/117

[58] **Field of Search** 359/53, 86, 40, 359/41, 48, 49, 50, 73

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Primary Examiner—William L. Sikes
Assistant Examiner—Tiep H. Nguyen
Attorney, Agent, or Firm—Longacre & White

[57] **ABSTRACT**

A double-layer type super-twisted nematic liquid crystal display system including a liquid crystal display device for displaying characters and/or graphic forms, a compensating liquid crystal device for compensating the optical phase of the liquid crystal display device, a temperature sensor for detecting the ambient temperature of those devices, a light sensor for calculation of the display contrast of the liquid crystal display device, drive voltage control circuits for controlling the drive voltages applied to the liquid crystal display device and the compensating liquid crystal device, and a displaying light source. In the display system, the drive voltages applied to the liquid crystal display device and compensating liquid crystal device are adjusted according to the calculation of contrast, whereby the display is high in contrast at all times independently of the ambient temperature.

7 Claims, 4 Drawing Sheets

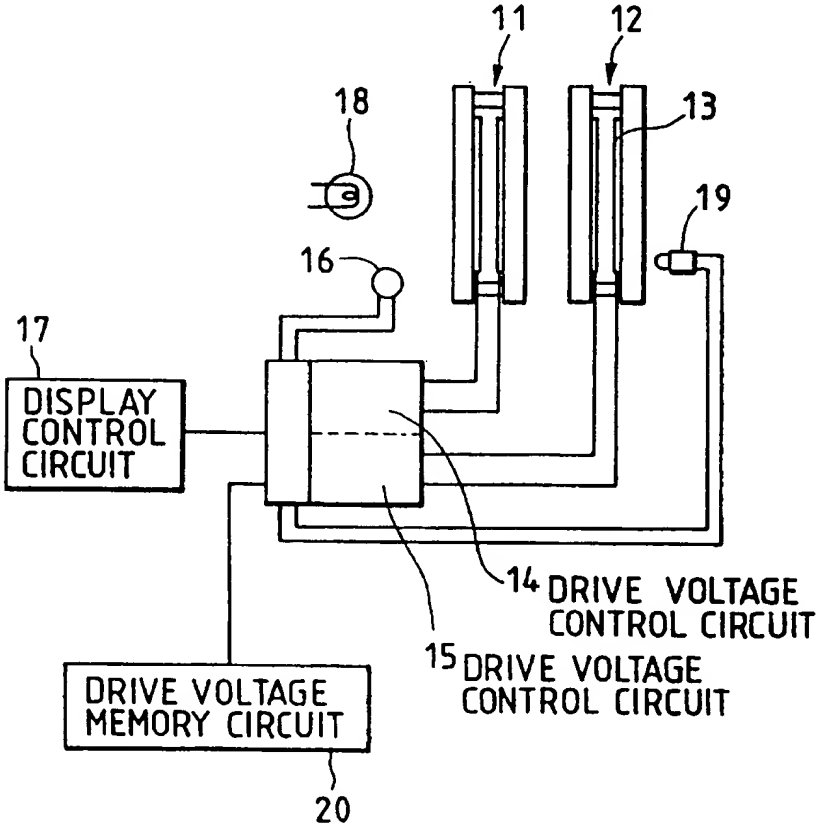


FIG. 1 PRIOR ART

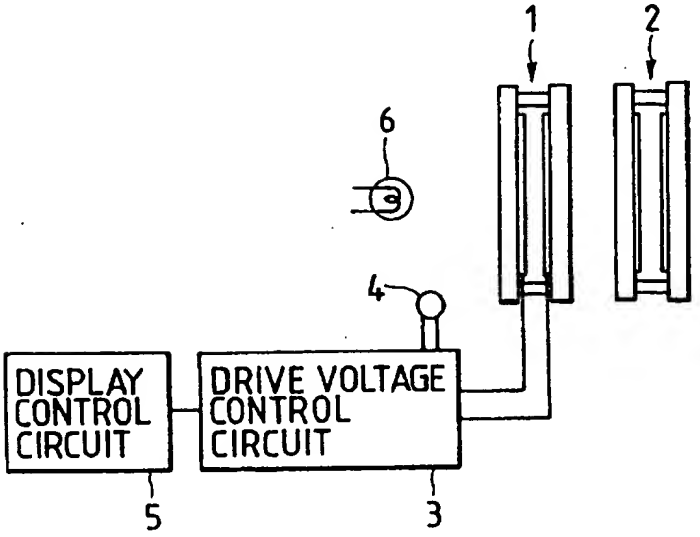


FIG. 2

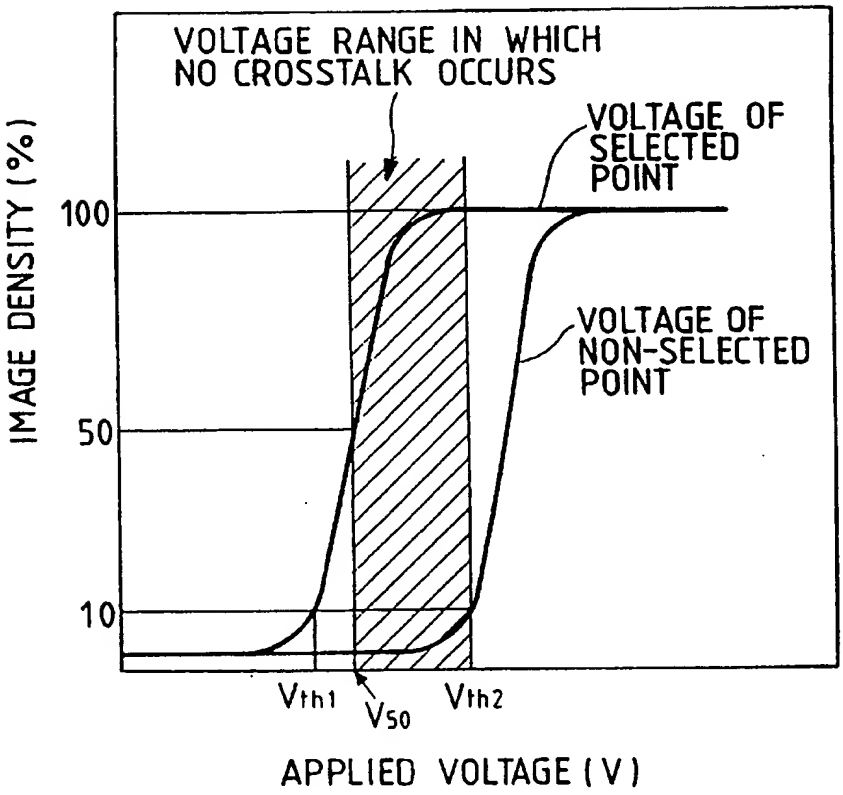


FIG. 3

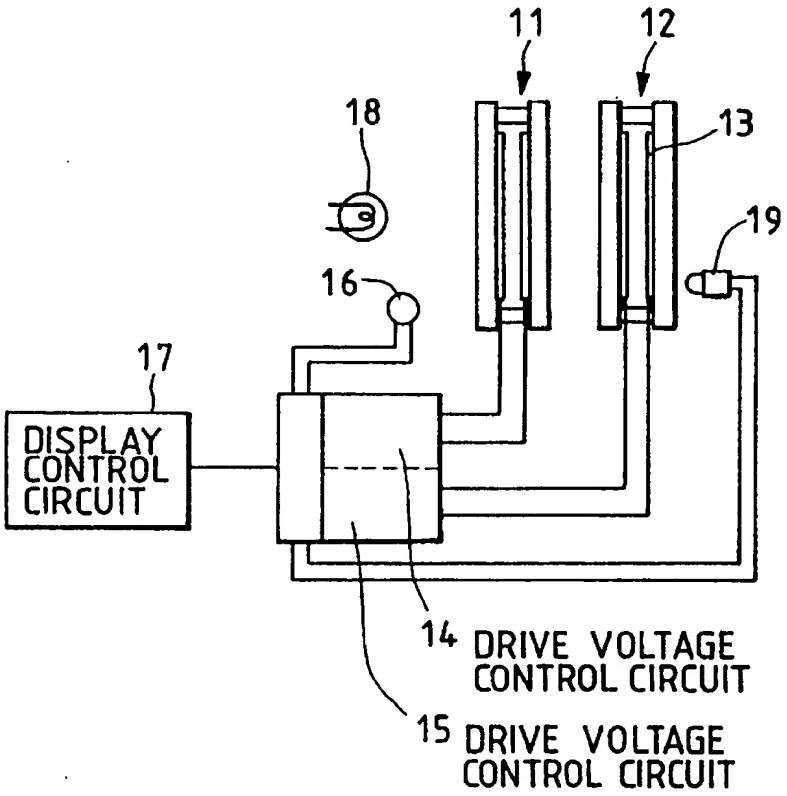

11
12
18
13
19
16
17
DISPLAY CONTROL CIRCUIT
14 DRIVE VOLTAGE CONTROL CIRCUIT
15 DRIVE VOLTAGE CONTROL CIRCUIT

FIG. 4

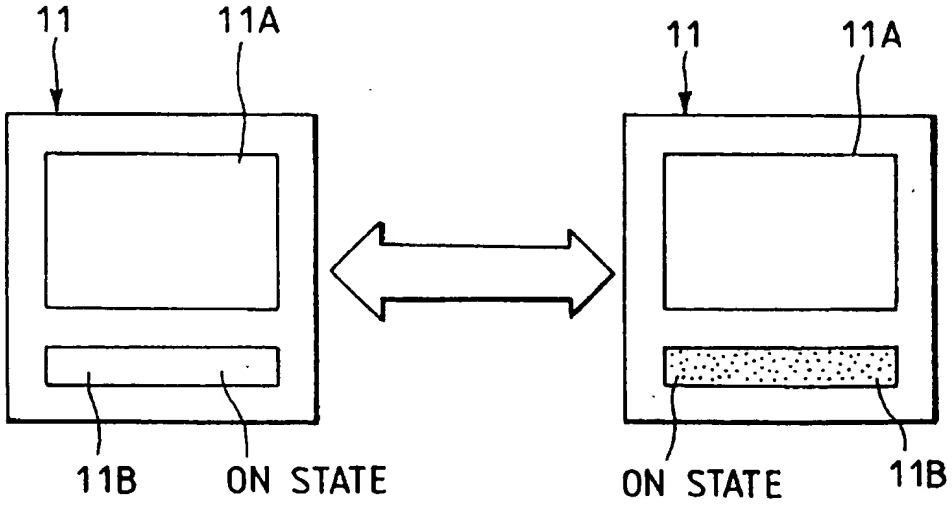

11
11A
11B
ON STATE
11
11A
ON STATE
11B

FIG. 5

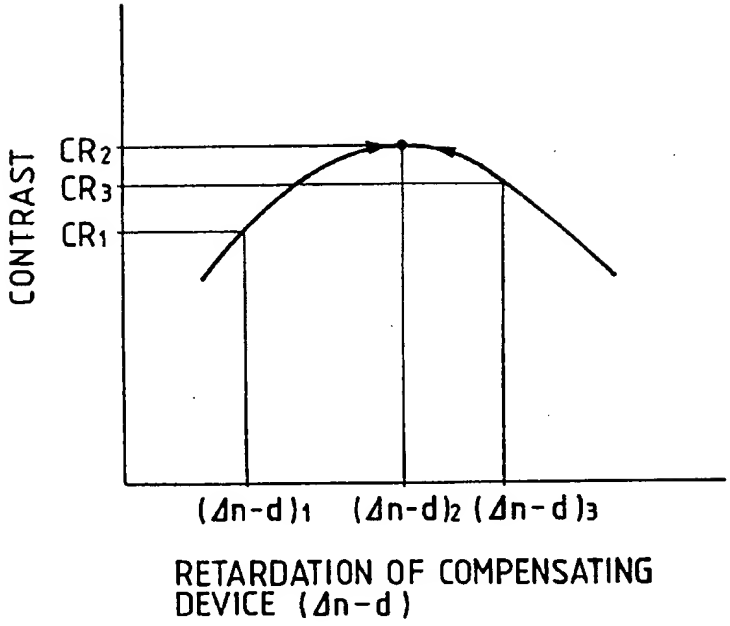

CONTRAST
CR2
CR3
CR1
(Δn-d)1
(Δn-d)2
(Δn-d)3
RETARDATION OF COMPENSATING DEVICE (Δn-d)

FIG. 6

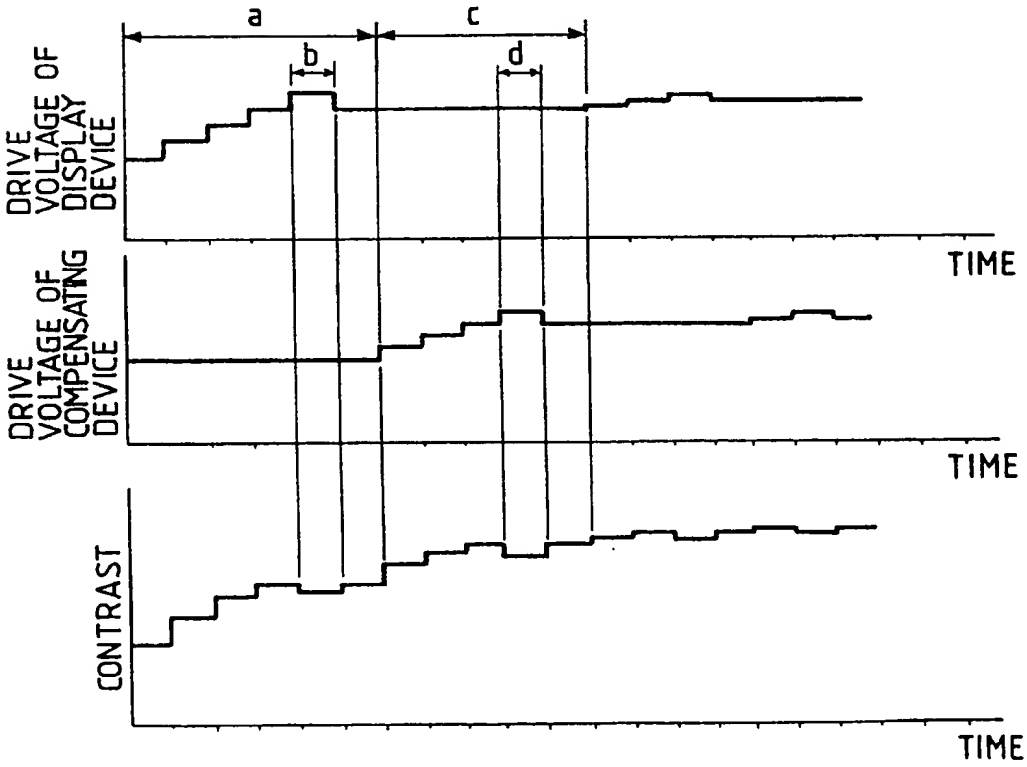

a
b
c
d
DRIVE VOLTAGE OF DISPLAY DEVICE
TIME
DRIVE VOLTAGE OF COMPENSATING DEVICE
TIME
CONTRAST
TIME

FIG. 7

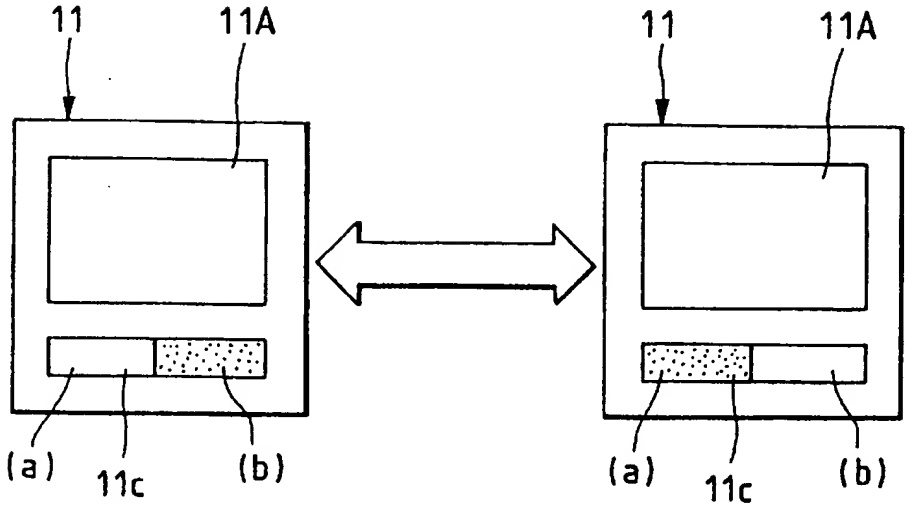
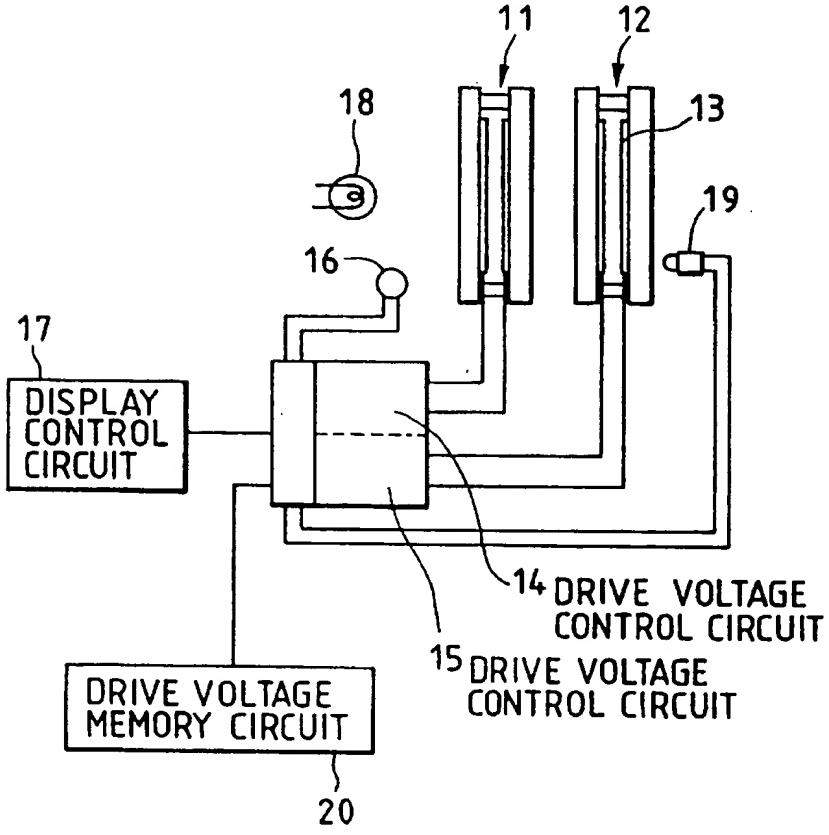

11
11A
11
11A
(a)
11c
(b)
(a)
11c
(b)

FIG. 8


11
12
18
13
19
16
17
DISPLAY CONTROL CIRCUIT
14 DRIVE VOLTAGE CONTROL CIRCUIT
15 DRIVE VOLTAGE CONTROL CIRCUIT
DRIVE VOLTAGE MEMORY CIRCUIT
20

LIQUID CRYSTAL DISPLAY SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a liquid crystal display system, and more particularly to a double-layer type super-twisted nematic liquid crystal display system.

2. Discussion of the Related Art

A conventional display means employed in an automobile's head-up display system is of a seven-segment type using fluorescent display tubes, because the display must be high in luminance. The fluorescent display tubes of the segments are selectively turned on to display, for instance, a vehicle speed and the number of revolutions per minute.

In the display means, the fluorescent display tubes emit light high in luminance. Hence, the display means is advantageously employed, for instance, for an automobile's head-up display system which makes display by reflecting light with a combiner. However, since the display means is of a seven-segment type, it is limited in the form of display; that is, what can be displayed by the display means is mainly numerical data. More specifically, it is unable for the display means to display a variety of data including characters and graphic forms. That is, the display means is rather inadequate as means for displaying a variety of pieces of information.

In order to eliminate this difficulty, a dot-matrix type transmission liquid crystal display device is employed as the display means in the head-up display system. In this case, in order to have a clear display, it is essential to use a liquid crystal display device which is able to provide a display sufficiently high in contrast.

There are available a variety of liquid crystal display devices, such as, a twist nematic type liquid crystal display device, a ferroelectric liquid crystal display device, and a phase transition type liquid crystal display device. Among those display devices, for instance, a super-twisted nematic liquid crystal device is considered to be relatively high in contrast. However, maximizing the display contrast of the super-twisted nematic liquid crystal device gives rise to various problems as follows:

FIG. **1** shows a conventional super-twisted nematic liquid crystal display system. The display system includes: a dot-matrix type super-twisted nematic liquid crystal display device (hereinafter referred to merely as "a liquid crystal display device", when applicable) **1**; and a compensating liquid crystal device **2**. The compensating liquid crystal device **2** optically eliminates a coloring phenomenon in the liquid crystal display device **1** which is caused by the phase difference in the direction of advance of light therein; that is, the device **2** makes the display monochromatic, thereby to increase the contrast. The twist angle of the compensating liquid crystal device **2** is opposite in direction to the twist angle of the liquid crystal display device **1**. The display system further includes: a drive voltage control circuit **3** for adjusting a drive voltage applied to the liquid crystal display device **1**; a temperature sensor **4** for detecting the ambient temperature of the liquid crystal display device **1**; a display control circuit **5** for allowing the liquid crystal display device **1** to display characters and/or graphic forms; and a light source **6** which irradiates the liquid crystal display device **1** in a transmission mode.

In the display system thus organized, in response to signals from the display control circuit **5**, the liquid crystal display device **1** displays characters and/or graphic forms.

The display on the display device **1** is irradiated by the output light of the light source **6** in a transmission mode. When the display thus irradiated passes through the compensating liquid crystal device **2**, the light twisted by the liquid crystal display device **1** is twisted back, which eliminates the elliptic light polarization attributing to the phase difference, and the variations in direction of the light polarization due to the wavelength of light. As a result, the display is made monochromatic; that is, the coloring phenomenon is eliminated, so that the display is improved in contrast.

In the conventional liquid crystal display system, the display (or image) on the liquid crystal display device **1** has a density characteristic as shown in FIG. **2**.

That is, in general, in order to make a display high in contrast, the following expressions must be satisfied:

$$V_{on} \geq V_{th} + \Delta V$$

$$V_{off} \geq V_{th}$$

where V_{th} is a threshold voltage with which the liquid crystal starts to provide an electro-optic effect, V_{on} is an effective voltage of a selected point (or a light-on picture element), and V_{off} is an effective voltage of a not-selected point (or a light-off picture element).

This will be described with reference to FIG. **2** in more detail.

As the applied voltage is gradually increased from zero, the selected point is increased in image density. When the applied voltage is further increased, the not-selected point is also increased in image density. If it is assumed that the selected point has an image density of 10% with a voltage V_{th1}, and an image density of 50% with a voltage V_{50}, and the not-selected point has an image density of 10% with a voltage V_{th2}, then the voltages with which an image high in contrast can be displayed are ranged from V_{50} to V_{th2}. This is generally called an "operating voltage range".

Thus, in order to improve the display contrast, the applied voltage should be set to a value in the above-described operating voltage range. On the other hand, in the case of a liquid crystal display system which is generally used, the above-described image density characteristic depends on the ambient temperature of the liquid crystal display device; that is, it is on the low voltage side when the ambient temperature increases, and it is on the high voltage side when the ambient temperature decreases. In order to overcome this difficulty, a temperature sensor such as a thermistor is employed to perform a temperature compensation according to the temperature characteristic of the drive voltage of the liquid crystal display device. However, since the temperature characteristic of the drive voltage is non-linear, the adjustment of the temperature characteristic by using the temperature sensor such as a thermistor is limited. On the other hand, the threshold voltage of the liquid crystal display device drifts, which makes it difficult to provide a suitable drive voltage, and accordingly to display a high contrast image.

SUMMARY OF THE INVENTION

Accordingly, an object of the invention is to eliminate the above-described difficulties accompanying a conventional liquid crystal display system.

More specifically, an object of the invention is to provide a liquid crystal display system in which the ambient temperature of the liquid crystal display device is detected, and the temperature thus detected is utilized to provide liquid crystal drive voltages with which the display made by the

liquid crystal display device and the compensating liquid crystal device provide are highest in contrast at all times independently of the ambient temperature.

In order to achieve the foregoing object, the invention provides a double-layer type super-twisted nematic liquid crystal display system including: a dot-matrix type liquid crystal display device for displaying at least one of characters and graphic forms; a compensating liquid crystal device, which has transparent electrodes for retardation adjustment, for compensating an optical phase of the liquid crystal display device; a display control circuit for causing the liquid crystal display device to display at least one of characters and graphic forms; a temperature sensor for detecting a temperature of an atmosphere in which the liquid crystal display device and the compensating liquid crystal device are set; light detecting means for measuring and calculating a display contrast of the liquid crystal display device; drive voltage control circuits for controlling drive voltages applied to the liquid crystal display device and the compensating liquid crystal device; and a displaying light source, wherein the liquid crystal display device and the compensating liquid crystal device are driven with drive voltages which are adjusted according to the calculation of contrast made with the aid of the light detecting means.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

FIG. **1** is an explanatory diagram showing the arrangement of a conventional liquid crystal display system;

FIG. **2** is a graphical representation indicating the image density characteristic of a liquid crystal display device in the conventional liquid crystal display system;

FIG. **3** is an explanatory diagram showing the arrangement of a liquid crystal display system, which constitutes a first embodiment of the invention;

FIG. **4** is an explanatory diagram for a description of a displaying operation performed by the liquid crystal display system shown in FIG. **3**;

FIG. **5** is a graphical representation indicating a contrast characteristic of a double-layer type super-twisted nematic liquid crystal display system;

FIG. **6** is a timing chart for a description of the control of voltages applied to the liquid crystal display device and the compensating liquid crystal device in the liquid crystal display system of the invention;

FIG. **7** is an explanatory diagram for a description of a modification of the first embodiment; and

FIG. **8** is an explanatory diagram showing the arrangement of another liquid crystal display system, which constitutes a second embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the invention will be described with reference to the accompanying drawings.

First Embodiment

A liquid crystal display system, which constitutes a first embodiment of the invention, as shown in FIG. **3**, includes: a dot-matrix type super-twisted nematic liquid crystal display device **11** (hereinafter referred to merely as "a liquid crystal display device", when applicable); a compensating liquid crystal device **12** laid over the front surface of the liquid crystal display device **11**, the device **12** having transparent electrodes **13** on its surface and having a twist angle which is opposite in direction to the twist angle of the liquid crystal display device **11**; a drive voltage control circuit **14** for adjusting a drive voltage applied to the liquid crystal display device **11**; and a drive voltage control circuit **15** for adjusting a drive voltage applied to the compensating liquid crystal device **12**. The display system further includes: a temperature sensor **16** for detecting the ambient temperature of the liquid crystal display device **11** to make liquid crystal driving voltages close to the values which are most suitable with the ambient temperature thus detected; a display control circuit **17** for displaying characters and graphic forms on the liquid crystal display device **11**; a light source **18** for irradiating the liquid crystal display device **11** in a transmission mode; and a photo sensor **19** for detecting the contrast of a display on the liquid crystal display device **11** observing it through the compensating liquid crystal device **12**.

The liquid crystal display device **11**, as shown in FIG. **4**, has a data display region **11A** for displaying data by using characters and graphic forms, and a luminance measuring region **11B**.

The liquid crystal display system thus organized operates as follows:

In response to a signal from the display control circuit **17**, characters and/or graphic forms are displayed in the display region **11A** of the liquid crystal display device **11**. The display in the region **11A** is irradiated, in a transmission mode, by the output light of the light source **18**. At the same time, the temperature sensor **16** detects the ambient temperature of the liquid crystal display device **11** (the temperature of the circumference where the display system is set), and a drive voltage most suitable for the liquid crystal display device **11**; i.e., a drive voltage which makes the contrast of the display on the liquid crystal display device **11** highest is determined from the ambient temperature thus detected.

In addition, when the liquid crystal display device **11** is driven, the ambient temperature of the latter **11** is detected by the temperature sensor **16**. On the other hand, while the luminance measuring region **11B** of the liquid crystal display device **11** being turned on and off with a suitable period as shown in FIG. **4**, the contrast thereof is measured with the photo sensor **19**, and the drive voltages of the liquid crystal display device **11** and the compensating liquid crystal device **12** are changed until liquid crystal panel drive voltages are obtained which make the contrast highest. This will be described in more detail.

In a double-layer type super-twisted nematic liquid crystal display system, the contrast is maximum when the retardation (that is an optical phase difference represented by the production of the difference Δn between two refractive indexes n_l and n_o of a liquid crystal molecule and the thickness of the liquid crystal layer—the inclination of the liquid crystal molecule, when regarded as a liquid crystal device, is changed in inclination depending on a voltage applied thereto, and the difference Δn of the liquid crystal device is changed, thus affecting the contrast) of the compensating liquid crystal device **12** is at $(\Delta n \cdot d)_2$ which is somewhat lower than the retardation $(\Delta n \cdot d)_3$ of the liquid crystal display device **11** (cf. FIG. **5**). The set retardation $(\Delta n \cdot d)$ of the compensating liquid crystal device **12** is generally different from the aimed value $(\Delta n \cdot d)_2$. Hence, even if the contrast of the display on the double-layer type super-twisted nematic liquid crystal display system is mea-

sured, and only the drive voltage for the liquid crystal display device is controlled, the maximum contrast cannot be obtained (cf. CR_1 and CR_3 in FIG. 5). Therefore, in the first embodiment, not only the drive voltage applied to the liquid crystal display device **11** but also the drive voltage applied to the compensating liquid crystal device **12** is changed to set the retardation of the latter **12** to the aimed value $(\Delta n \cdot)_2$, thereby to obtain the maximum contrast CR_2.

The voltage control of the liquid crystal display device **11** and the compensating liquid crystal device **12** will be described with reference to FIGS. **3** and **6**.

First, drive voltages corresponding to an ambient temperature detected by the temperature sensor **16** are applied to the liquid crystal display device **11** and the compensating liquid crystal device **12**.

Under this condition, while the contrast of the display on the double-layer type super-twisted nematic liquid crystal display system is being measured, the drive voltage of the liquid crystal display device **11** is increased or decreased (in the case of FIG. **6**, the drive voltage is increased) with the drive voltage of the compensating liquid crystal device **12** maintained constant (a in FIG. **6**). If this operation decreases the contrast (b in FIG. 6), then the drive voltage of the liquid crystal display device **11** is changed to the preceding value which it had immediately before the operation. Next, similarly as in the above-described operation, while the contrast is being measured, the drive voltage of the compensating crystal liquid device **12** is increased or decreased (in the case of FIG. **6**, the drive voltage is increased) with the drive voltage of the liquid crystal display device **11** maintained constant (c in FIG. **6**). If this operation decreases the contrast (d in FIG. **6**), the drive voltage of the compensating liquid crystal device **12** is returned to the preceding value which it had immediately before the operation.

The above-described operations are repeatedly carried out. As a result, the drive voltages of the double-layer type super-twisted nematic liquid crystal system are so controlled that the contrast is maximum at all times irrespective of the ambient temperatures.

FIG. **7** shows a modification of the above-described first embodiment. The modification is obtained by replacing the luminance measuring region **11B** of the first embodiment with a luminance measuring region **11C** which is designed as follows: The luminance measuring region **11C** is divided into two parts, namely, a right part (b) and a left part (a) which are alternately turned on and off with a predetermined period. That is, when the right part (b) is turned on, the left part (a) is turned off; and vice versa. In addition, two photo sensors **19** are provided for those two parts (a) and (b), respectively.

The reason why the right and left parts of the luminance measuring region **11C** are turned on and off with the predetermined period is to eliminate a difficulty accompanying a liquid crystal display system, especially a super-twisted nematic liquid crystal display system, that, if the same display is kept for a long time, a so-called "burning" occurs with the region, so that the region becomes different in display characteristic from the other regions. In addition, the reason why the luminance measuring region **11C** is divided into the two parts (a) and (b) is to measure the luminance of the two parts in "on"0 and "off" states at the same time, thereby to quickly obtain the most suitable contrast.

If summarized, in the liquid crystal display system designed as described above, the most suitable contrast is obtained as follows: The luminance measuring region **11B** (or **11C**) of the liquid crystal display device **11** is turned on and off with a suitable period, and the luminances of the luminance measuring region which is in "on" state and in "off" state are measured with the photo sensor **19** (or the photo sensors **19**). Then, the drive voltage applied to the liquid crystal display device **11** is controlled so that the ratio of the luminances thus measured; that is, the contrast be maximum. Hence, even if the liquid crystal display device **11** is varied in characteristic when manufactured, or when used for a long time, or the ambient temperature of the liquid crystal display device **11** is variable, the drive voltage of the liquid crystal display device **11** is controlled according to those variations, so that the best contrast is obtained at all times.

Second Embodiment

Another liquid crystal display system, which constitutes a second embodiment of the invention, will be described with reference to FIG. **8**.

As is apparent from comparison of FIGS. **3** and **8**, the second embodiment is obtained by adding a drive voltage memory circuit **20** to the first embodiment described above.

The liquid crystal display system operates as follows: Similarly as in the case of the first embodiment shown in FIG. **3**, when the liquid crystal display device **11** is driven, the ambient temperature of the latter **11** is detected with the temperature sensor **16**. On the other hand, while the luminance measuring region **11B** of the liquid crystal display device **11** being turned on and off with a suitable period, the contrast thereof is measured with the photo sensor **19**, and the drive voltages applied to the liquid crystal display device **11** and the compensating liquid crystal device **12** are changed until liquid crystal panel drive voltages are obtained which make the contrast maximum. Furthermore, in the second embodiment, the liquid crystal drive voltages thus obtained are stored in the drive voltage memory circuit **20**.

In addition, the drive voltages, which make the contrast maximum with respect to each ambient temperature of the liquid crystal display device, are stored in the drive voltage memory circuit **20** in a renewal mode.

The drive voltages thus stored are used as initial drive voltages when the liquid crystal display system is driven later, so that the highest contrast can be quickly and automatically obtained. This feature is effective in practical use as follows: In the case where the display is made with the luminance of the light source reduced for instance at night, it is difficult to accurately detect the luminance of the luminance measuring region, especially when it is in "off" state (in dark state), as a result of which the calculation of the contrast is greatly lowered in accuracy, which makes it impossible to control the drive voltages according to the result of the calculation. In this case, the latest drive voltage data corresponding to the present temperature are read out of the drive voltage memory circuit **20**, so that suitable drive voltages are applied to the liquid crystal display device **11** and the compensating liquid crystal device **12**. Thus, even when the display is made with a small quantity of light, its most suitable contrast can be quickly obtained.

As was described above, in the double-layer type super-twisted nematic liquid crystal display system including: the dot-matrix type liquid crystal display device **11** for displaying characters and/or graphic forms; and the compensating liquid crystal device **12** for compensating the optical phase of the device **11**, the compensating liquid crystal device **12** also has transparent electrodes for retardation adjustment.

The display system further includes: the temperature sensor **16** for detecting the temperature of an atmosphere in which the liquid crystal display device and the compensating liquid crystal device are set; the photo sensor **19** for measuring and calculating the display contrast of the liquid crystal display device; the drive voltage control circuits **14** and **15** for controlling drive voltages applied to the liquid crystal display device **11** and the compensating liquid crystal device **12**; and the displaying light source **18**. In the display system thus organized, drive voltages applied to the liquid crystal display device **11** and the compensating liquid crystal device **12** are adjusted according to the calculation of contrast. Hence, even if the liquid crystal display device **11** and the compensating liquid crystal device **12** are varied in characteristic when manufactured, or when used for a long time, or the ambient temperature of those devices **11** and **12** changes, the drive voltages applied to the devices **11** and **12** are adjusted according to those variations, so that the display is best in contrast at all times.

Furthermore, the double-layer type super-twisted nematic liquid crystal display system, according to another aspect of the invention, further includes: the memory circuit **20** for storing drive voltages applied to the liquid crystal display device and the compensating liquid crystal device with respect to the ambient temperatures of those devices. Hence, in the case where it is difficult to perform the contrast calculation because it is low in the quantity of light, the drive voltage data stored with respect to the temperatures are read out of the memory circuit **20** so that suitable drive voltages are applied to the liquid crystal display device **11** and the compensating liquid crystal device **12**. That is, even when it is low in the quantity of light, the display is best in contrast. When the liquid crystal display device is operated again later, the drive voltage data stored in the memory circuit in a renewal mode may be employed as initial drive voltage data. Thus, in driving the liquid crystal display device again, the best contrast can be obtained quickly.

While there has been described in connection with the preferred embodiments of this invention, it will be obvious to those skilled in the art that various changes and modifications may be made therein without departing from the invention, and it is aimed, therefore, to cover in the appended claim all such changes and modifications as fall within the true spirit and scope of the invention.

What is claimed is:

1. A double-layer type super-twisted nematic liquid crystal display system comprising:

a dot-matrix type liquid crystal display device for displaying at least one of characters and graphic forms;

a compensating liquid crystal device, which has transparent electrodes for retardation adjustment, for compensating an optical phase of said liquid crystal display device;

a display control circuit for causing said liquid crystal display device to display at least one of characters and forms;

a temperature sensor for detecting a temperature of an atmosphere in which said liquid crystal display device and said compensating liquid crystal device are set, to provide an initial optimum value range for one or more drive voltages;

light detecting means for measuring and calculating a display contrast of said liquid crystal display device;

at least two drive voltage control circuits for controlling said drive voltages, said drive voltages applied to said liquid crystal display device and said compensating device; and

a displaying light source,

wherein said liquid crystal display device and said compensating liquid crystal device are driven with said drive voltages which are adjusted according to the calculation of contrast made with the aid of said light detecting means.

2. A double-layer type super twisted nematic liquid crystal display system according to claim **1**, further comprising:

a voltage memory circuit for storing most recent values of said drive voltages while said system is an off state to provide initial drive voltage values for when said system is switched to an on state.

3. A double-layer type super-twisted nematic liquid crystal display system comprising:

a dot-matrix type liquid crystal display device for displaying at least one of characters and graphic forms;

a compensating liquid crystal device, which has transparent electrodes for retardation adjustment, for compensating an optical phase of said liquid crystal display device;

a display control circuit for causing said liquid crystal display device to display at least one of characters and forms;

a temperature sensor for detecting a temperature of an atmosphere in which said liquid crystal display device and said compensating liquid crystal device are set, to provide an initial optimum value range for one or more drive voltages:

light detecting means for measuring and calculating a display contrast of said liquid crystal display device;

drive voltage control circuits for controlling said drive voltages, said drive voltages applied to said liquid crystal display device and said compensating device; and

a displaying light source,

wherein said liquid crystal display device and said compensating liquid crystal device are driven with said drive voltages which are adjusted according to the calculation of contrast made with the aid of said light detecting means and said liquid crystal display has a luminance measuring region which is turned on and off for measurement of the contrast of said liquid crystal display device.

4. A double layer type super-twisted nematic liquid crystal display system comprising:

a dot-matrix type liquid crystal display device for displaying at least one of characters and graphic forms;

a compensating liquid crystal device, which has transparent electrodes for retardation adjustment, for compensating an optical phase of said liquid crystal display device;

a display control circuit for causing said liquid crystal display device to display at least one of characters and forms;

a temperature sensor for detecting a temperature of an atmosphere in which said liquid crystal display device and said compensating liquid crystal device are set, to provide an initial optimum value range for one or more drive voltages;

light detecting means for measuring and calculating a display contrast of said liquid crystal display device;

drive voltage control circuits for controlling said drive voltages, said drive voltages applied to said liquid crystal display device and said compensating device; and

a displaying light source,

wherein said liquid crystal display device and said compensating liquid crystal device are driven with said drive voltages which are adjusted according to the calculation of contrast made with the aid of said light detecting means and said liquid crystal display device has a luminance measuring region which is divided into two parts which are alternately turned on and off for measurement of the contrast of said liquid crystal display device.

5. A double layer type super-twisted nematic liquid crystal display system comprising:

a dot-matrix type liquid crystal display device for displaying at least one of characters and graphic forms;

a compensating liquid crystal device, which has transparent electrodes for retardation adjustment, for compensating an optical phase of said liquid crystal display device;

a display control circuit for causing said liquid crystal display device to display at least one of characters and forms;

a temperature sensor for detecting a temperature of an atmosphere in which said liquid crystal display device and said compensating liquid crystal device are set, to provide an initial optimum value range for one or more drive voltages;

light detecting means for measuring and calculating a display contrast of said liquid crystal display device;

drive voltage control circuits for controlling said drive voltages, said drive voltages applied to said liquid crystal display device and said compensating device; and

a memory circuit for storing data on drive voltages applied to said liquid crystal display device and said compensating liquid crystal device with respect to the temperatures thus detected; and

a displaying light source,

wherein the drive voltages applied to said liquid crystal display device and said compensating liquid crystal device are adjusted according to the calculation of contrast made with the aid of said light detecting means, and when a quantity of light required for the calculation of light required for the calculation of contrast is insufficient, the data on drive voltages stored in said memory circuit are selectively utilized to drive said liquid crystal display device and said compensating liquid crystal device.

6. The liquid crystal display system as claimed in claim 5, wherein said liquid crystal display device has a luminance measuring region which is turned on and off for measurement of the contrast of said liquid crystal display device.

7. The liquid crystal display system as claimed in claim 5, wherein said liquid crystal display device has a luminance measuring region which is divided into two parts which are alternately turned on and off for measurement of the contrast of said liquid crystal display device.

* * * * *

APPENDIX D

Koyama Reference

U.S. Patent No. 6,310,598

US006310598B1

(12) **United States Patent**
Koyama et al.

(10) **Patent No.: US 6,310,598 B1**
(45) **Date of Patent: Oct. 30, 2001**

(54) **MATRIX TYPE LIQUID-CRYSTAL DISPLAY UNIT**

(75) Inventors: **Jun Koyama**, Kanagawa; **Shunpei Yamazaki**, Tokyo, both of (JP)

(73) Assignee: **Semiconductor Energy Laboratory Co., Ltd.**, Kanagawa-ken (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/474,939**

(22) Filed: **Dec. 30, 1999**

Related U.S. Application Data

(63) Continuation of application No. 09/300,716, filed on Apr. 27, 1999, now Pat. No. 6,037,924, which is a continuation of application No. 08/730,409, filed on Oct. 15, 1996, now Pat. No. 5,956,011.

(30) **Foreign Application Priority Data**

Oct. 14, 1995 (JP) 7-291765

(51) **Int. Cl.**[7] **G09G 3/36**

(52) **U.S. Cl.** **345/98**; 345/90; 345/92; 345/96; 345/100; 345/204; 345/211; 345/212; 323/313

(58) **Field of Search** 345/90, 92, 96, 345/98, 100, 204, 211, 212; 323/313

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6,037,924	*	3/2000	Koyama et al.	345/92

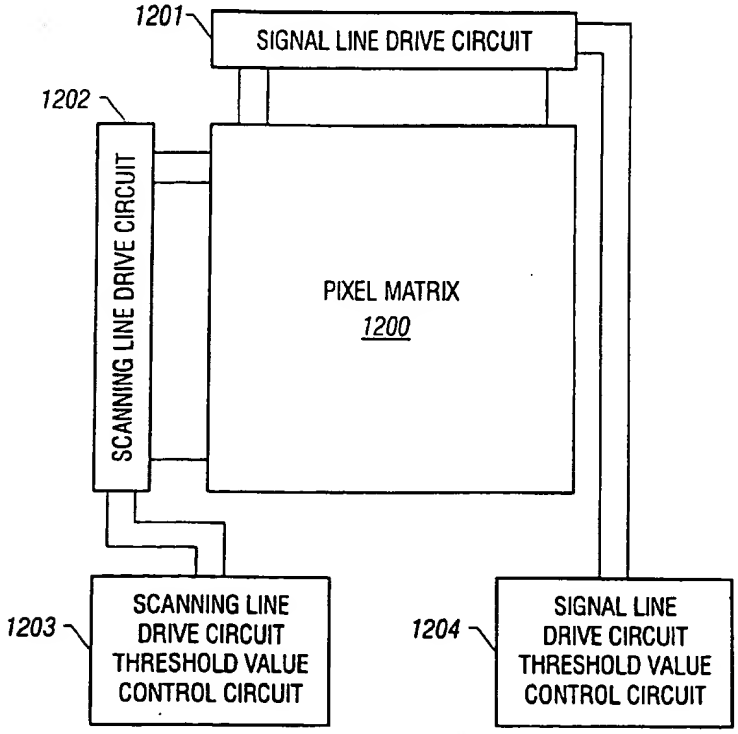
* cited by examiner

Primary Examiner—Bipin Shalwala
Assistant Examiner—Vincent E. Kovalick
(74) *Attorney, Agent, or Firm*—Fish & Richardson P.C.

(57) **ABSTRACT**

A matrix type liquid-crystal display unit includes: a plurality of pixel portions which are arranged in the form of a matrix; a plurality of signal lines through which a display signal is supplied to the pixel portions; a plurality of scanning lines through which a scanning signal is supplied to the pixel portions; a signal-line drive circuit for driving the signal lines; a scanning-line drive circuit for driving the scanning-lines; a plurality of first thin-film transistors that form the signal-line drive circuit; a plurality of second thin-film transistors that form the scanning-line drive circuit; and a threshold value control circuit being connected to the signal-line drive circuit and the scanning-line drive circuit, for commonly controlling threshold values of the first and second thin-film transistors.

15 Claims, 10 Drawing Sheets



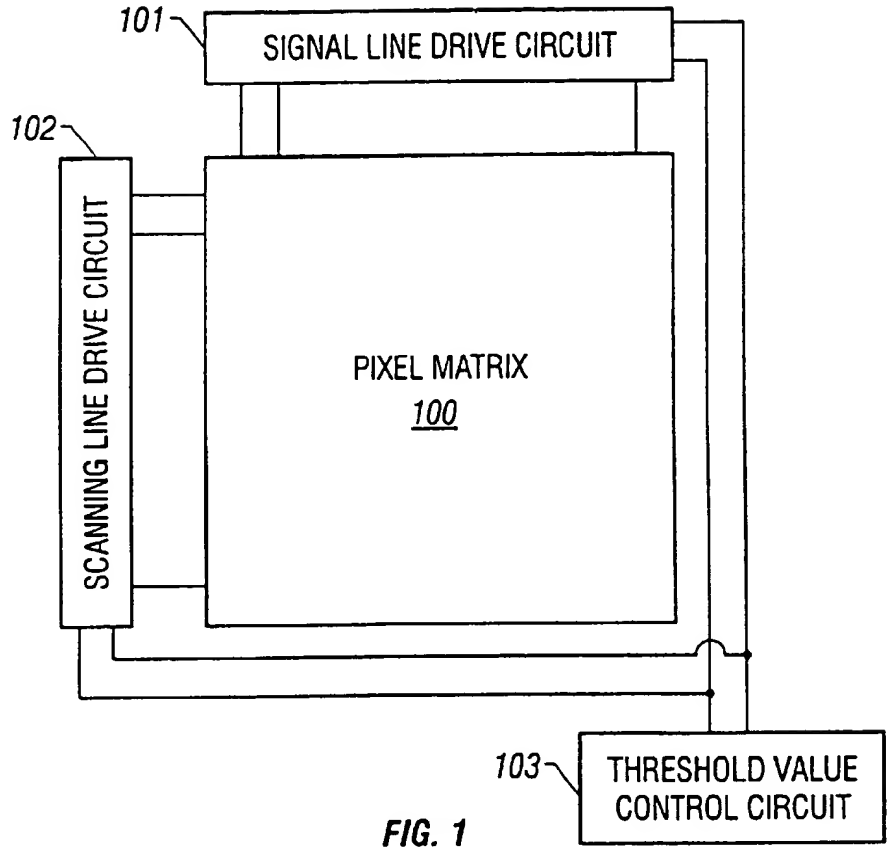

101
SIGNAL LINE DRIVE CIRCUIT
102
SCANNING LINE DRIVE CIRCUIT
PIXEL MATRIX
100
103
THRESHOLD VALUE CONTROL CIRCUIT

FIG. 1

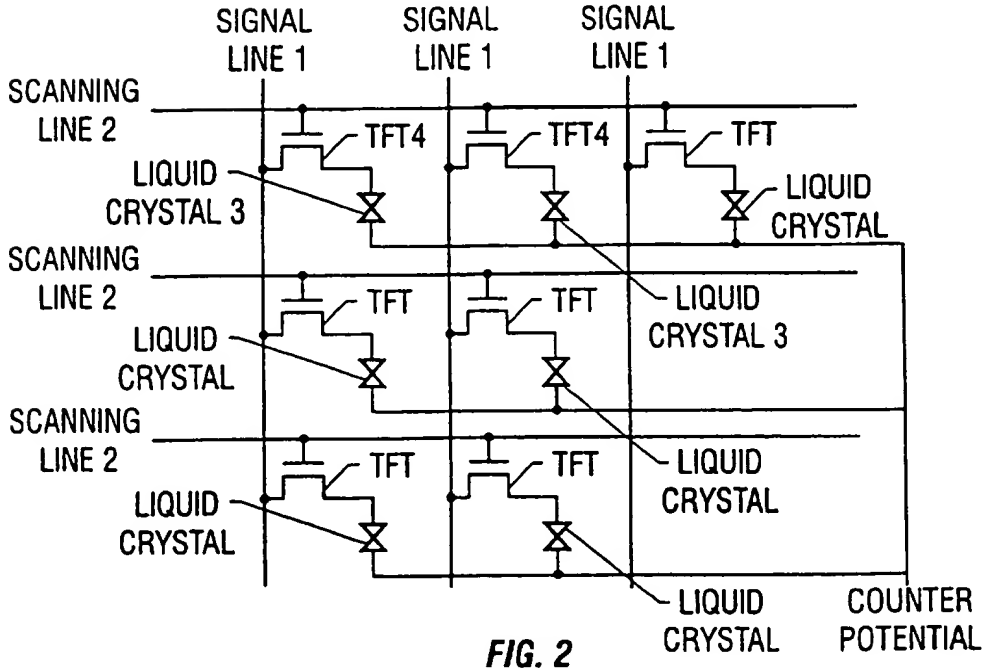

SIGNAL LINE 1
SIGNAL LINE 1
SIGNAL LINE 1
SCANNING LINE 2
SCANNING LINE 2
SCANNING LINE 2
TFT4
TFT4
TFT
TFT
TFT
TFT
LIQUID CRYSTAL 3
LIQUID CRYSTAL
LIQUID CRYSTAL
LIQUID CRYSTAL
LIQUID CRYSTAL 3
LIQUID CRYSTAL
LIQUID CRYSTAL
LIQUID CRYSTAL
COUNTER POTENTIAL

FIG. 2

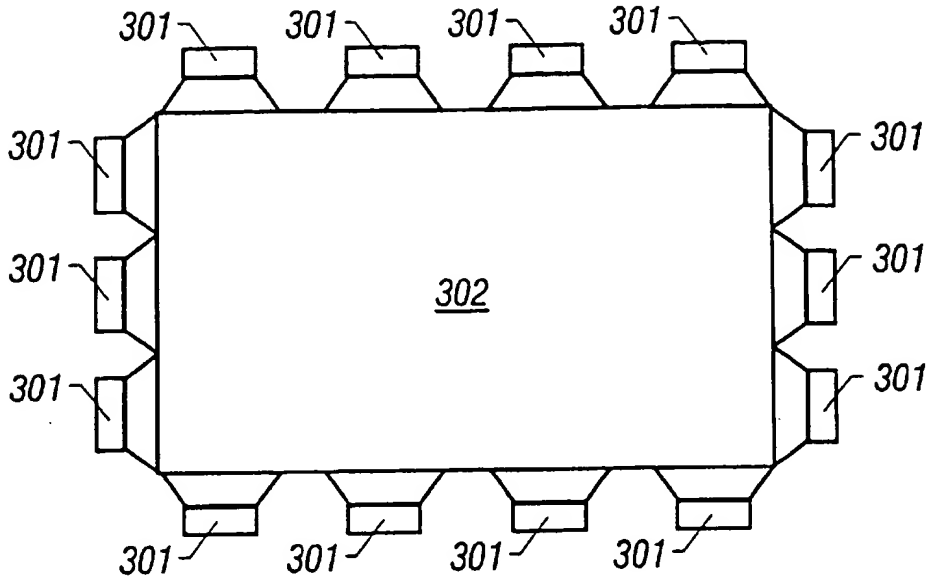

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FIG. 3A

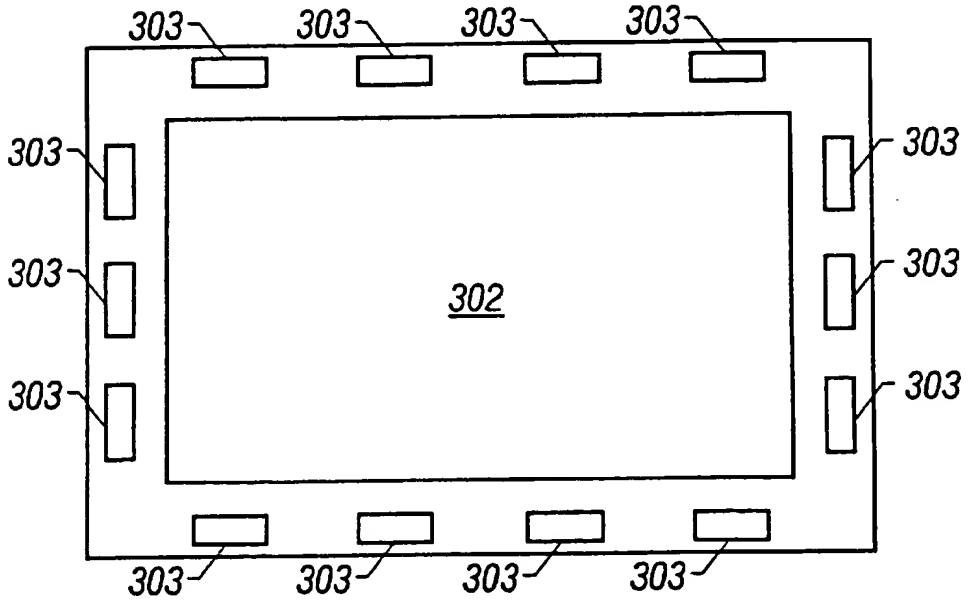
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FIG. 3B

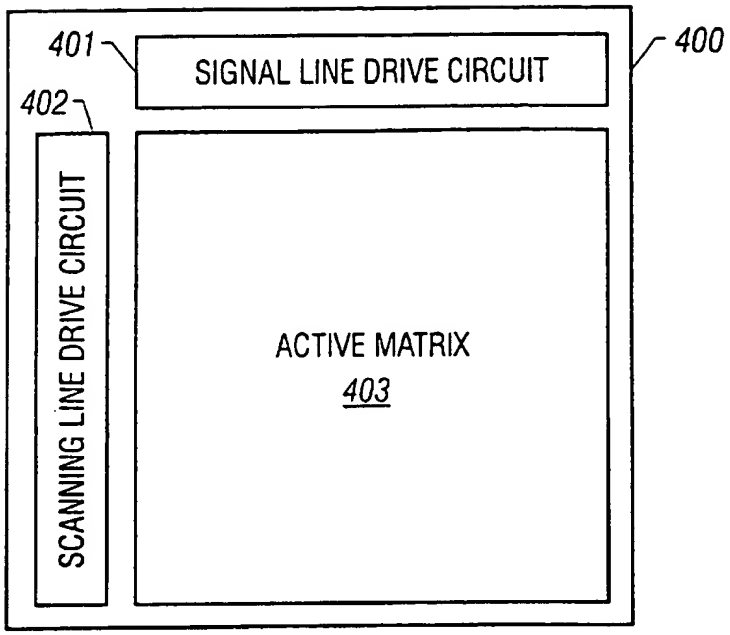
401
SIGNAL LINE DRIVE CIRCUIT
400
402
SCANNING LINE DRIVE CIRCUIT
ACTIVE MATRIX
403

FIG. 4A

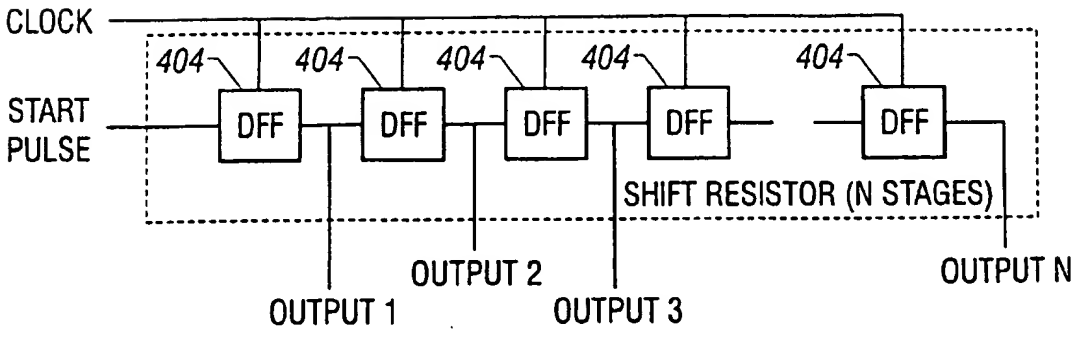
CLOCK
START PULSE
404
DFF
SHIFT RESISTOR (N STAGES)
OUTPUT 1
OUTPUT 2
OUTPUT 3
OUTPUT N

FIG. 4B

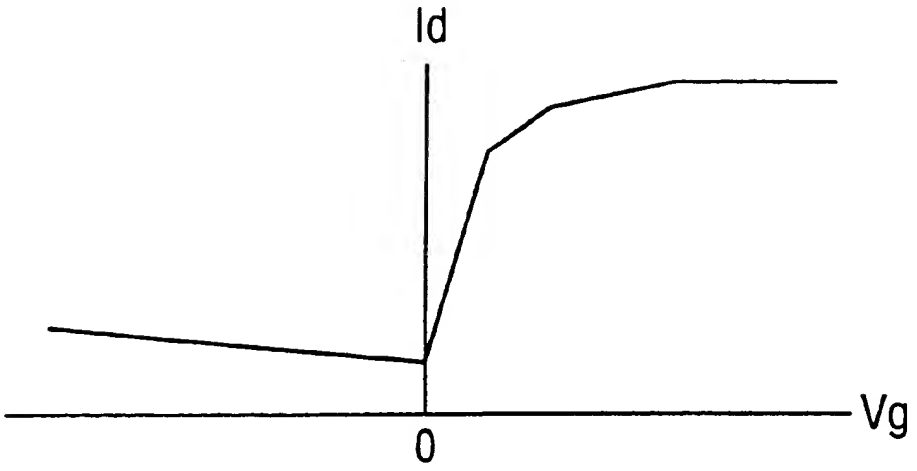

FIG. 5A

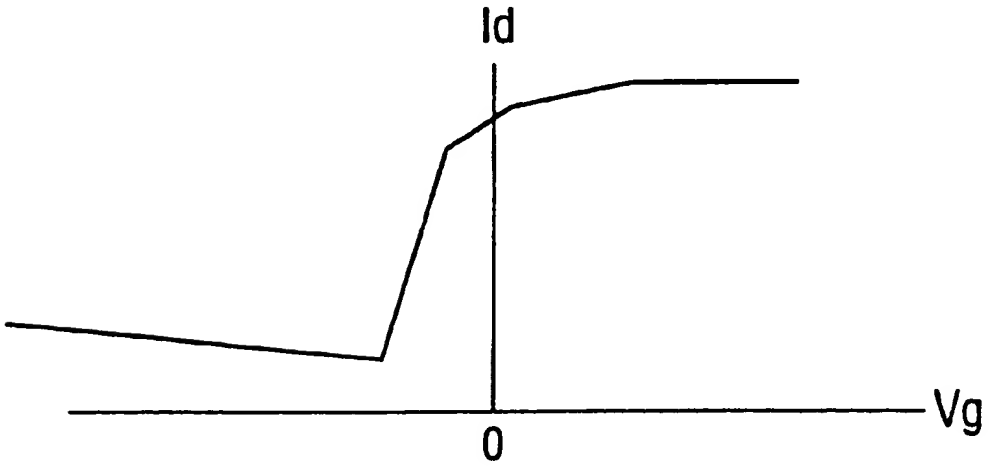

FIG. 5B

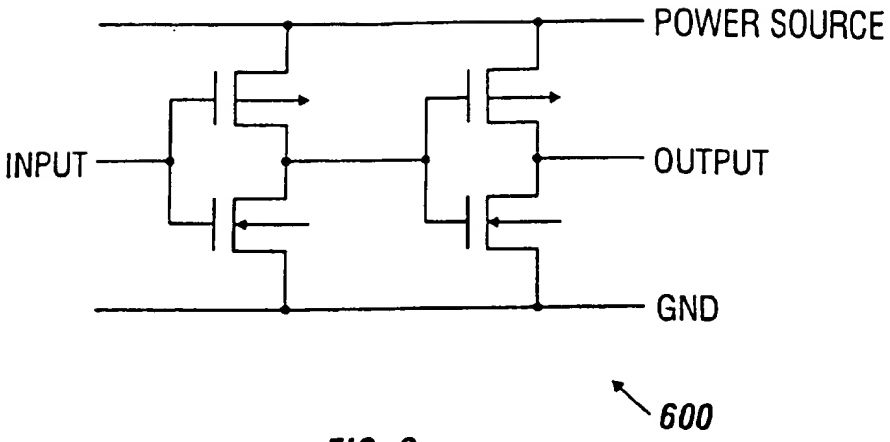
POWER SOURCE
INPUT
OUTPUT
GND
600

FIG. 6

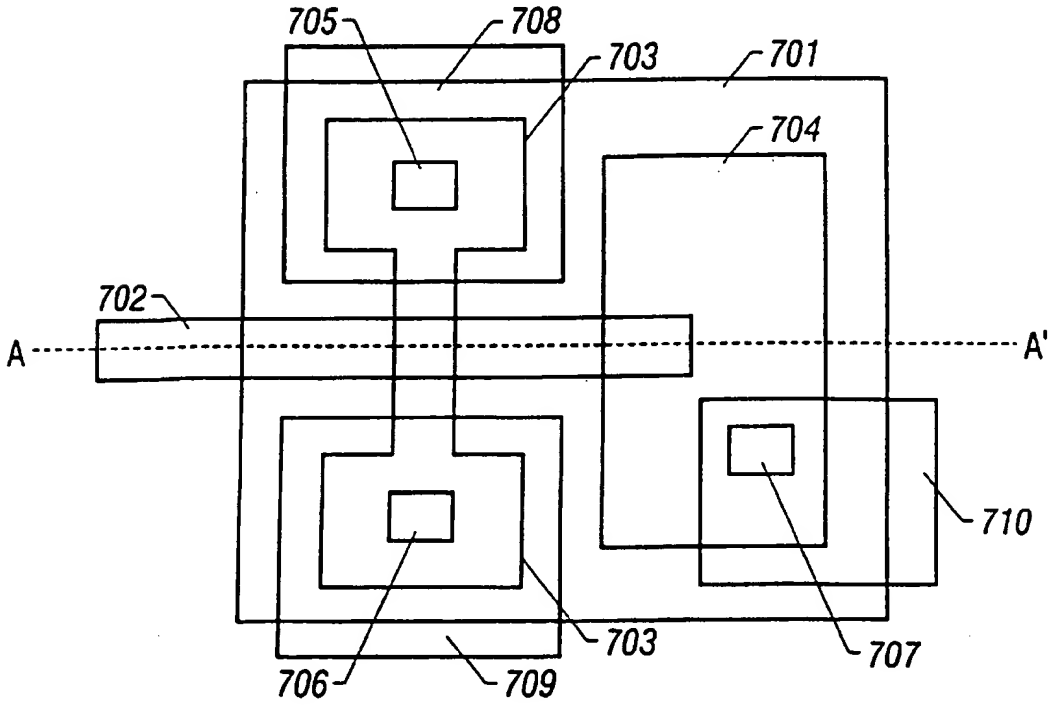
705
708
703
701
704
702
A
A'
710
703
706
709
707

FIG. 7

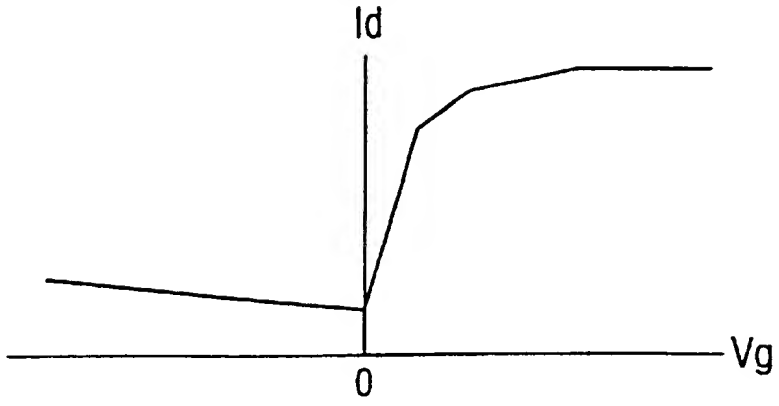

FIG. 8A

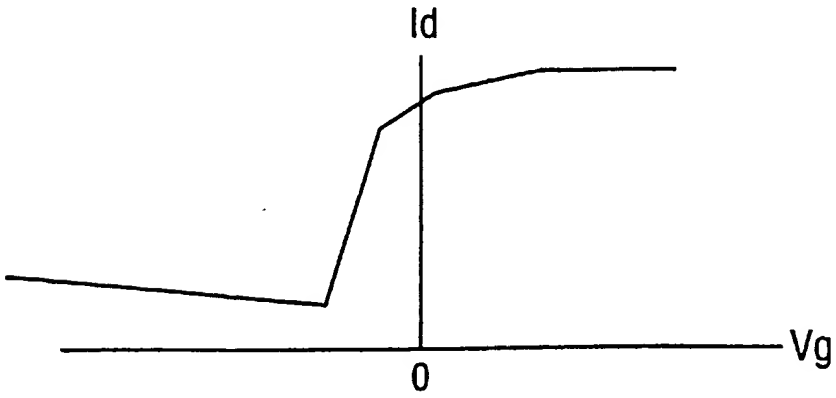

FIG. 8B

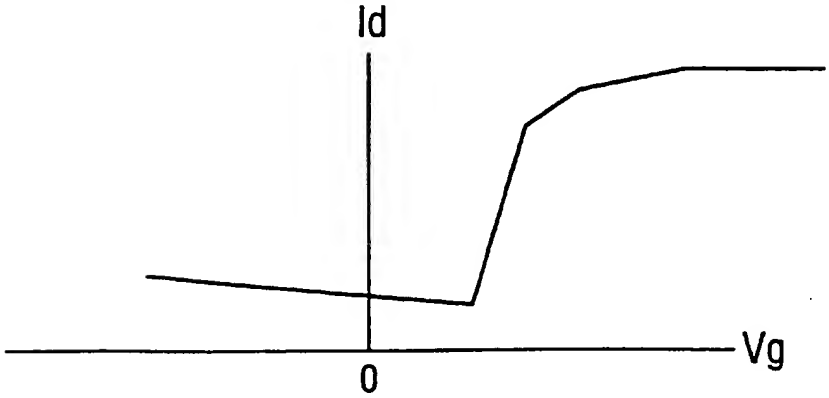

FIG. 8C

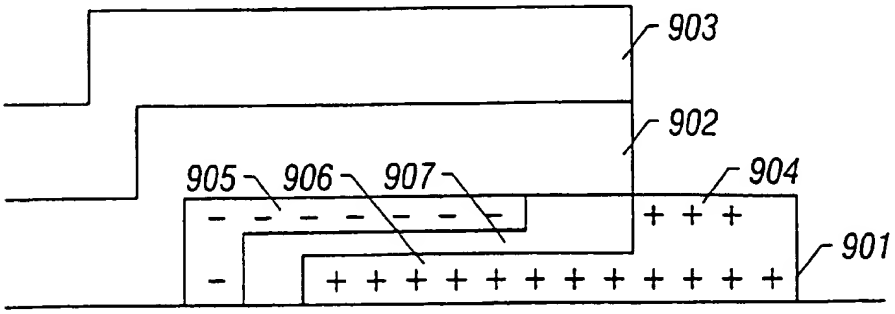
903
902
905
906
907
904
901

FIG. 9

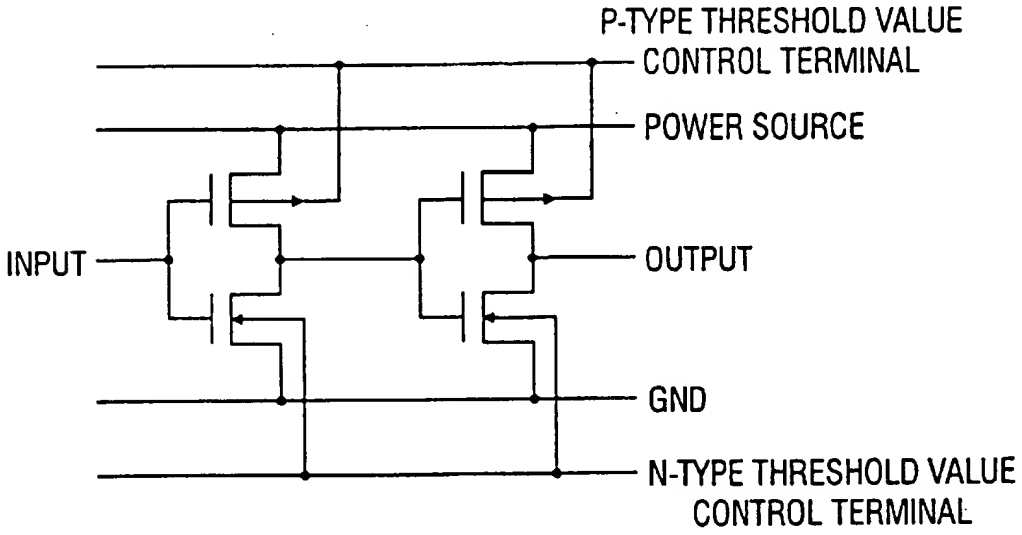
P-TYPE THRESHOLD VALUE CONTROL TERMINAL
POWER SOURCE
INPUT
OUTPUT
GND
N-TYPE THRESHOLD VALUE CONTROL TERMINAL

FIG. 10

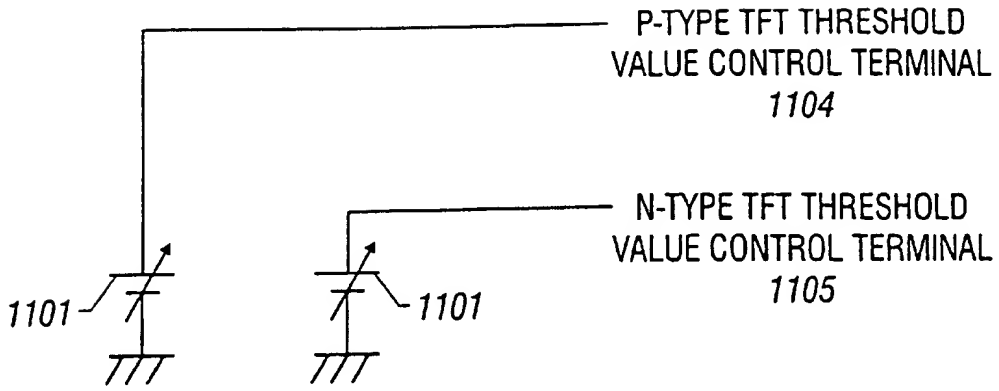

FIG. 11A

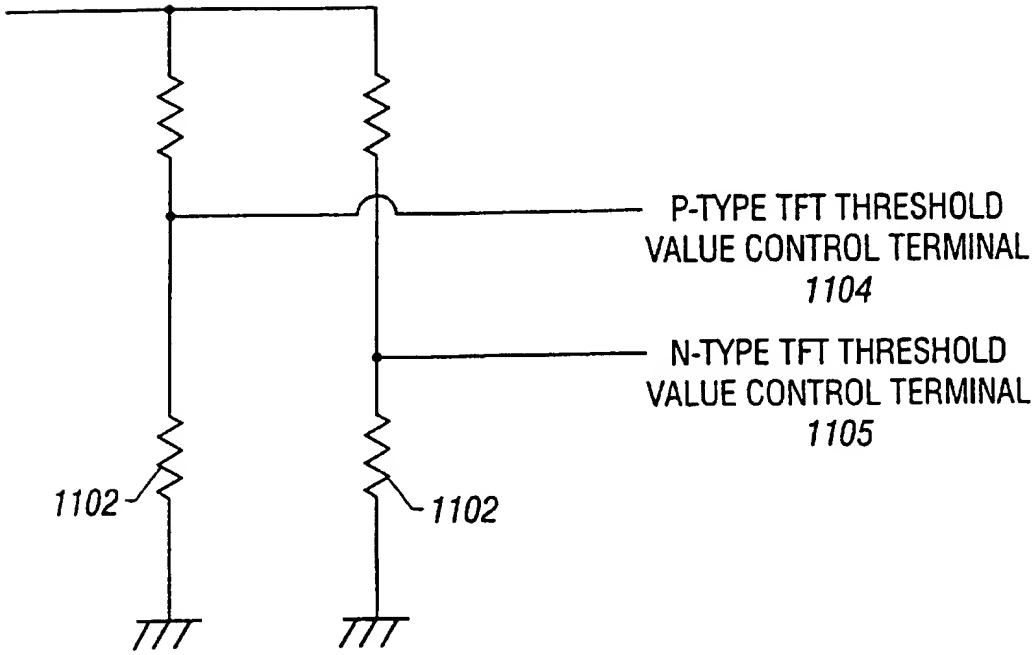

FIG. 11B

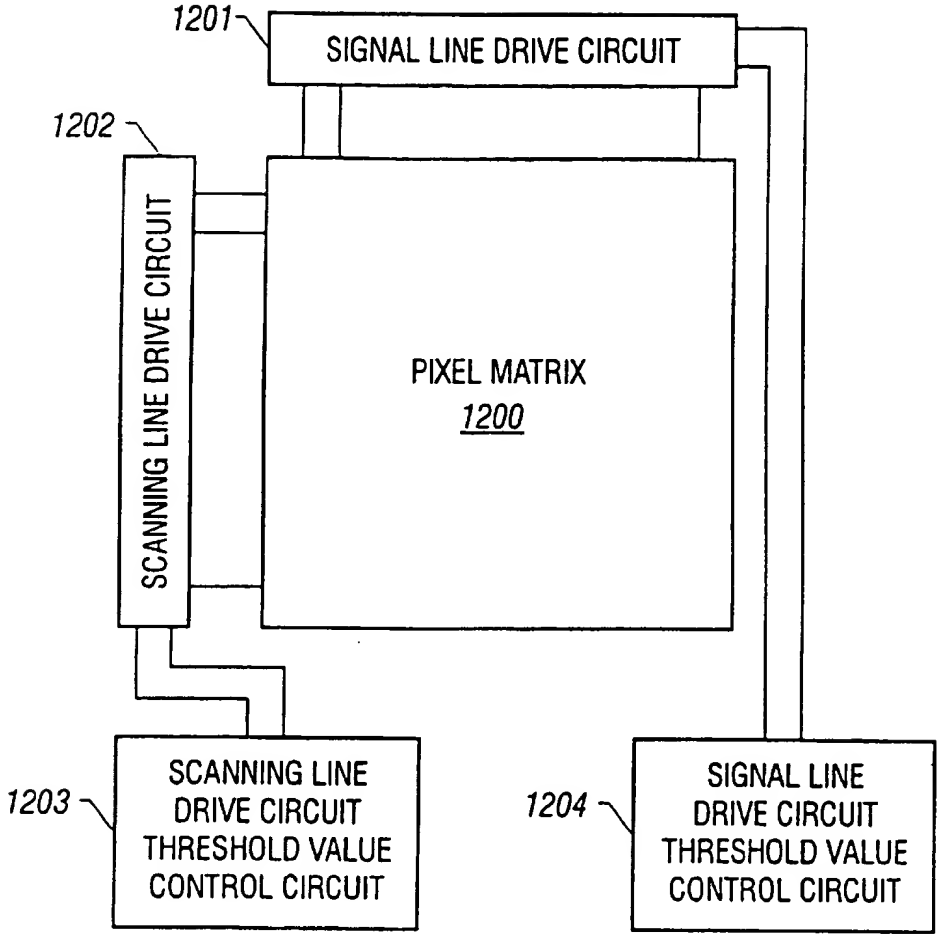
1201
SIGNAL LINE DRIVE CIRCUIT
1202
SCANNING LINE DRIVE CIRCUIT
PIXEL MATRIX
1200
1203
SCANNING LINE DRIVE CIRCUIT THRESHOLD VALUE CONTROL CIRCUIT
1204
SIGNAL LINE DRIVE CIRCUIT THRESHOLD VALUE CONTROL CIRCUIT

FIG. 12

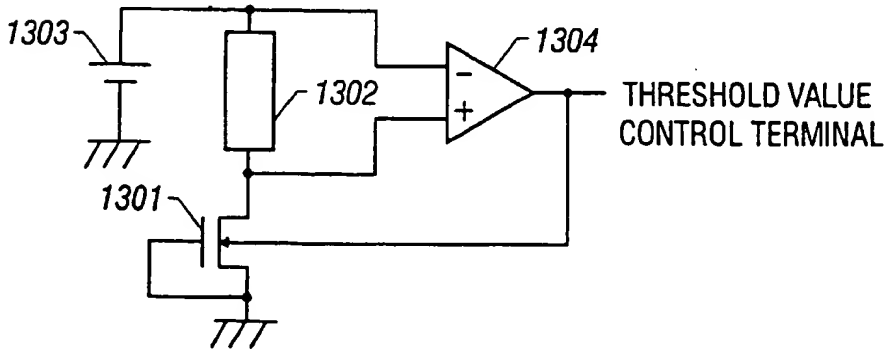
1303
1302
1304
THRESHOLD VALUE CONTROL TERMINAL
1301

FIG. 13

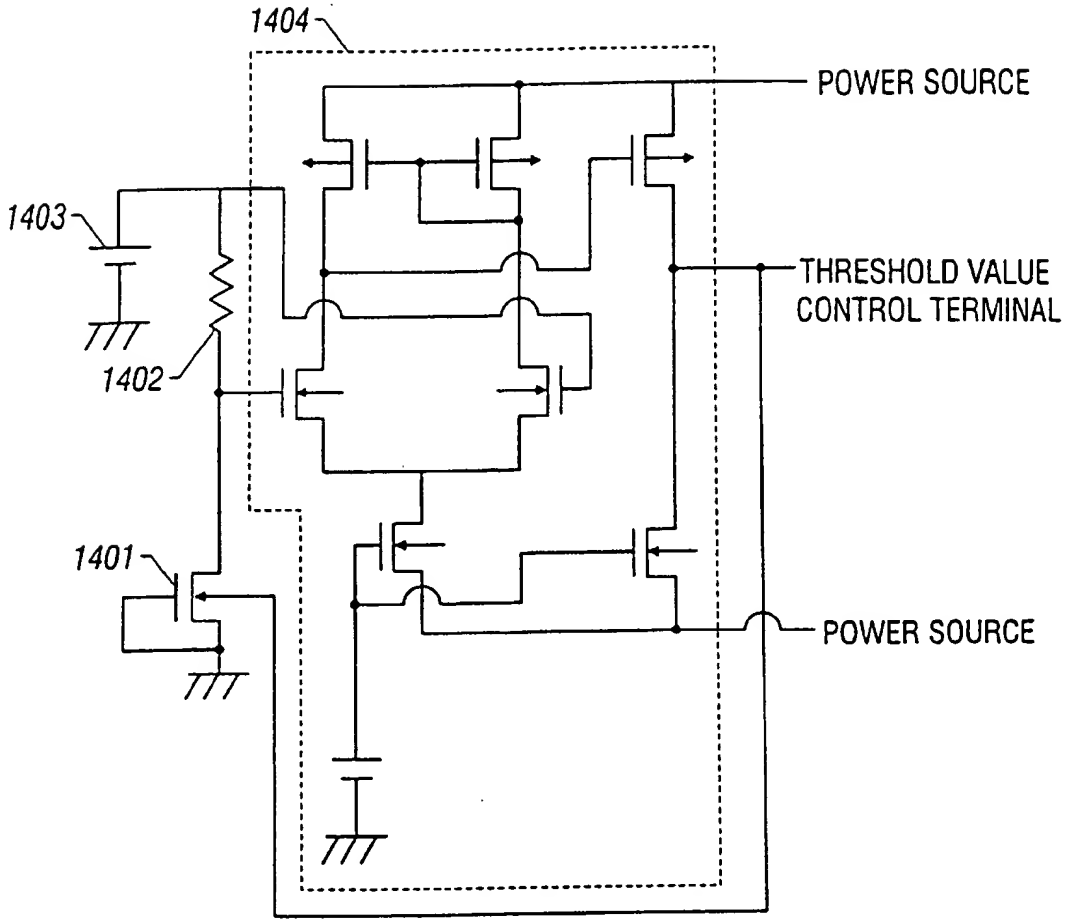
1404
POWER SOURCE
1403
THRESHOLD VALUE
CONTROL TERMINAL
1402
1401
POWER SOURCE

FIG. 14

MATRIX TYPE LIQUID-CRYSTAL DISPLAY UNIT

This is a continuation of U.S. application Ser. No. 09/300,716, filed Apr. 27, 1999 U.S. Pat. No. 6,037,924, which is a continuation of U.S. application Ser. No. 08/730,409, filed Oct. 15, 1996, U.S. Pat. No. 5,956,011.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a matrix type display unit, and more particularly to a matrix type display unit containing a drive circuit therein.

2. Description of the Related Art

The active matrix type display unit is a display unit in which a pixel is arranged at each intersection of a matrix which is made up of signal lines **1** and scanning lines **2**, and a switching element is provided for each pixel in such a manner that pixel information is controlled by turning on/off the respective switching elements, as shown in FIG. **2**. Liquid crystal **3** is used as a display medium of the display unit of this type. The switching element may be formed of, in particular, a three-terminal element, that is, a thin-film transistor **4** having a gate, a source and a drain.

Also, in the present specification, a "row" in the matrix is defined by the scanning line **2** (gate line), which is arranged in parallel to a subject row, being connected to a gate electrode of the thin-film transistor **4** of the subject row, and a "column" in the matrix is defined by the signal line **1** (source line), which is arranged in parallel to a subject row, being connected to a source (or drain) electrode of the thin-film transistor **4** of the subject column. Furthermore, a circuit that drives the scanning line **2** is called a "scanning line drive circuit", and a circuit that drives the signal line **1** is called a "signal line drive circuit". Also, the thin-film transistor is called a "TFT".

What is shown in FIG. **3** is a first conventional example of the active matrix type liquid-crystal display unit. The active matrix type liquid-crystal display unit of this example has the TFT using amorphous silicon, and the scanning line drive circuits and the signal line drive circuits which are made up of monocrystal integrated circuits (**301**, **303**), and they are fitted onto the periphery of a glass substrate using tabs as shown in FIG. **3A**, or the former are fitted onto the latter through the COG (chip on glass) technique as shown in FIG. **3B**.

The liquid-crystal display unit of this type suffers from problems stated below. One problem may arise from the viewpoint of the reliability because the signal lines and the scanning lines of the active matrix are connected to each other through the tabs or bonding wire. For example, in the case where the display unit is of VGA (video graphic array), the number of signal lines is 1920, and the number of scanning lines is 480. The number of those lines shows a tendency to increase year by year as the resolution is improved.

In the case of producing a video camera view finder or a projector using liquid crystal, there is required that the display unit is compacted in a lump. The liquid-crystal display unit using the tabs as shown in FIG. **3A** is disadvantageous from the viewpoint of a space.

There has been developed the active matrix type liquid-crystal display unit that solves those problems in which TFT is made of polysilicon. One example of this display unit is shown in FIGS. **4A** and **4B**. As shown in FIG. **4A**, a signal line drive circuit **401** and a scanning line drive circuit **402** are formed on a glass substrate **400** together with pixel TFTs of an active matrix **403**, using polysilicon TFTs. The formation of the polysilicon TFT is conducted by a high-temperature polysilicon process in which an element is formed on a quartz substrate through a process at 1000° C. or higher, or a low-temperature polysilicon process in which an element is formed on a glass substrate through a process at 600° C. or lower.

The polysilicon TFT can increase its mobility to 30 $cm^2/Vsec$ or more whereas the amorphous TFT is about 0.5 $cm^2/Vsec$ in mobility. Thus, polysilicon TFT can be operated by a signal of about severals MHz.

The drive circuit that drives the active matrix type liquid-crystal display unit is of the digital type and the analog type. The drive circuit using polysilicon is generally of the analog type. It should be noted that because the number of elements in the circuit of the digital type is remarkably more than that of the analog type, the drive circuit using polysilicon is generally of the analog type. Also, the circuit structure of the scanning line drive circuit and the signal line drive circuit generally uses a shift register **405** in which N- delay type flip flop circuits **404** are connected in series (refer to FIG. **4B**).

The above-described conventional liquid-crystal display unit suffers from problems stated below. In the TFT using polysilicon, the control of a threshold value is generally difficult in comparison with a monocrystal transistor, and what is naturally to be of the enhancement type becomes of the depletion type so that a current may flow into a drain even though a voltage between a gate and a source is 0. This is because polysilicon is nonuniform in crystallinity more than monocrystal, a thermal oxide film cannot be used for a gate oxide film in the case of the low-temperature polysilicon, impurity contamination is caused, and so on.

For example, assuming that the TFT characteristic which is to be naturally exhibited by FIG. **5A** becomes the characteristic shown in FIG. **5B** with a shift of the threshold value, in an initial stage of an invertor circuit **600** shown in FIG. **6**, no current flows when an input signal is in a high-state, but a current is caused to flow from a power supply to GND when the input signal is in a low-state. Further, current flows in the next stage in a high condition. Also, in the case where the drive circuit for the liquid-crystal display unit is installed in a substrate of a TFT, its stage number becomes 1120 in total at both of a signal side and a scanning side when the display unit is of the VGA type. As a result, even though a small current flows into each of the TFTs, the total value of the current becomes large. This causes a serious problem from the viewpoint of reducing a power consumption of the display unit.

On the other hand, if the threshold value becomes too large, an on-state current of the TFT is decreased, resulting in such a problem that the operating frequency of the drive circuit is lowered. The operating frequency of the drive circuit is determined by the magnitude of the on-state current when a load capacity and a supply voltage are kept constant because the load capacity is driven by the on-state current of the TFT. Hence, the too large threshold value leads to a lowered operating frequency.

SUMMARY OF THE INVENTION

The present invention has been made in view of the above problems with the conventional display unit, and therefore an object of the present invention is to provide a matrix type display unit that controls the threshold value of TFTs by the application of a voltage, thereby reducing a power consump-

tion of a drive circuit or improving the operating frequency of the drive circuit.

In order to achieve the above object, according to a first aspect of the present invention, there is provided a matrix type liquid-crystal display unit, which comprises: a plurality of pixel portions which are arranged in the form of a matrix; a plurality of signal lines through which a display signal is supplied to said pixel portions; a plurality of scanning lines through which a scanning signal is supplied to said pixel portions; a drive circuit for driving at least one of said signal lines and said scanning lines; a plurality of thin-film transistors that form said drive circuit; and a threshold value control circuit being connected to said drive circuit for controlling a threshold value of said thin-film transistors.

According to a second aspect of the present invention, each of said thin-film transistors includes a control terminal through which the threshold value of said thin-film transistors is controlled, and said threshold value control circuit applies a desired voltage to said control terminal.

According to a third aspect of the present invention, said control terminal is formed in a channel contact region which is connected to a channel of said thin-film transistor, and said threshold value control circuit applies the desired voltage to said control terminal to change the channel, thus controlling the threshold value.

According to a fourth aspect of the present invention, the conductive type of said channel contact region is opposite to that of the channel of said thin-film transistors during operation thereof. Said channel contact region is p-type in case that the channel is n-type. Said channel contact region is n-type in case that the channel is p-type.

According to a fifth aspect of the present invention, said threshold value control circuit applies a voltage lower than a ground potential in order to reduce the power consumption of said drive circuit when said thin-film transistor is of the n-type.

According to a sixth aspect of the present invention, said threshold value control circuit applies a voltage higher than a supply potential in order to reduce the consumption power of said drive circuit when said thin-film transistor is of the p-type.

According to a seventh aspect of the present invention, said threshold value control circuit applies a voltage higher than a ground potential in order to improve the operating frequency of said drive circuit when said thin-film transistor is of the n-type.

According to an eighth aspect of the present invention, said threshold value control circuit applies a voltage lower than a supply potential in order to improve the operating frequency of said drive circuit when said thin-film transistor is of the p-type.

According to a ninth aspect of the present invention, said threshold value control circuit includes a variable resistor and adjusts the resistance of the variable resistor to apply the desired voltage to said control terminal.

According to a tenth aspect of the present invention, said threshold value control circuit includes a monitoring thin-film transistor that includes a threshold value control terminal for setting a reference value; a load for converting a current that flows in said monitoring thin-film transistor into a voltage; and an amplifier for amplifying a voltage developed across said load to apply an amplified voltage to said drive circuit, and to negatively feed back the amplified voltage to said threshold value control terminal of said monitoring thin-film transistor.

According to an eleventh aspect of the present invention, said threshold value control circuit is formed of a thin-film transistor on a substrate commonly used for that of said drive circuit.

According to a twelfth aspect of the present invention, said thin-film transistor is of a complementary transistor pair made up of an n-type transistor and a p-type transistor, the n-type transistor is provided with a first control terminal, the p-type transistor is provided with a second control terminal, and said threshold value control circuit applies desired voltages to the first and second control terminals, respectively.

According to a thirteenth aspect of the present invention, there is provided a liquid-crystal display unit, which comprises: a plurality of pixel portions which are arranged in the form of a matrix; a plurality of signal lines through which a display signal is supplied to said pixel portions; a plurality of scanning lines through which a scanning signal is supplied to said pixel portions; a signal-line drive circuit for driving said signal lines; a scanning-line drive circuit for driving said scanning-lines; a plurality of first thin-film transistors that form said signal-line drive circuit; a plurality of second thin-film transistors that form said scanning-line drive circuit; and a threshold value control circuit being connected to said signal-line drive circuit and said scanning-line drive circuit, for commonly controlling threshold values of said first and second thin-film transistors.

According to a fourteenth aspect of the present invention, there is provided a liquid-crystal display unit, which comprises: a plurality of pixel portions which are arranged in the form of a matrix; a plurality of signal lines through which a display signal is supplied to said pixel portions; a plurality of scanning lines through which a scanning signal is supplied to said pixel portions; a signal-line drive circuit for driving said signal lines; a scanning-line drive circuit for driving said scanning-lines; a plurality of first thin-film transistors that form said signal-line drive circuit; a plurality of second thin-film transistors that form said scanning-line drive circuit; a first threshold value control circuit being connected to said signal-line drive circuit, for controlling a threshold value of said first thin-film transistors; and a second threshold value control circuit being connected to said scanning-line drive circuit, for controlling a threshold value of said second thin-film transistors independently of said first threshold value control circuit.

According to a fifteenth aspect of the present invention, said first threshold value control circuit controls the threshold value so as to improve the operating frequency of said signal-line drive circuit, and said second threshold value control circuit controls the threshold value so as to reduce the power consumption of said scanning-line drive circuit.

In the liquid-crystal display unit of the present invention, the pixel portions are arranged in the form of a matrix, and there is provided the drive circuit for driving the signal lines through which the display signal is supplied to the pixel portions or the scanning lines through which the scanning signal is supplied to the pixel portions. The drive circuit is made up of a plurality of thin-film transistors. The drive circuit is connected with the threshold value control circuit for controlling the threshold value of the thin-film transistors. In the present invention, the threshold value control circuit is so designed as to control the threshold value of the thin-film transistors, thereby reducing the power consumption of the drive circuit or improving the operating frequency.

Each of the thin-film transistors is provided with the control terminal through which the threshold value is con-

trolled. The threshold value control circuit applies to the desired voltage to the control terminal. Specifically, each of the control terminals is formed in the channel contact region which is connected to the channel of each thin-film transistor, and the threshold value control circuit applies the desired voltage to the control terminal to change the channel, thus controlling the threshold value.

The channel contact region is opposite in conductive type to the channel of said thin-film transistors. For example, when said thin-film transistors are of the n-type, the channel contact region is of the p-type. In this case, the channel contact region is formed by doping the region with p-type impurities. In this manner, the thin-film transistors each having the control terminal are formed with such a structure, upon applying a voltage to the control terminal by the threshold value control circuit, the channel contact region functions as a so-called back gate, thereby influencing the channel of the thin-film transistor. As a result, the threshold value of the thin-film transistor can be controlled.

In this situation, the applied voltage is different between a case in which the power consumption of the drive circuit is to be reduced and a case in which the operating frequency is to be improved. Furthermore, the applied voltage depends on the polarity of the thin-film transistors. Specifically, when the thin-film transistors are of the n-type, a voltage lower than a ground potential is applied to the control terminal in order to reduce the consumption power of said drive circuit, or a voltage higher than the ground potential is applied to the control terminal in order to improve the operating frequency. On the other hand, when the thin-film transistors are of the p-type, a voltage higher than a supply voltage is applied to the control terminal in order to reduce the consumption power of said drive circuit, or a voltage lower than the supply voltage is applied to the control terminal in order to improve the operating frequency.

It should be noted that the control of the threshold value may be conducted by monitoring a current value of the drive circuit or a current value of the individual thin-film transistors, or automatically conducted by conducting the negative feedback. In the former case, the variable resistor is disposed in the threshold value control circuit so that the resistance of the variable resistor is adjusted, thus applying the desired voltage to the control terminal.

In the latter case, the threshold value control circuit may include the monitoring thin-film transistor for setting a reference value, the load for converting a current that flows in the monitoring thin-film transistor into a voltage, and the amplifier for amplifying a voltage developed across the load to apply an amplified voltage to the drive circuit and to negatively feed back the amplified voltage to the threshold value control terminals of the monitoring thin-film transistors. In the latter case, it is preferable that the threshold value control circuit is formed of a thin-film transistor on a substrate commonly used for that of the drive circuit.

Also, in the case where the thin-film transistors are of a complementary transistor pair (CMOS), the n-type transistor is provided with the first control terminal, the p-type transistor is provided with the second control terminal, so that the threshold value control circuit applies desired voltages to the first and second control terminals, respectively.

Also, the drive circuit includes the signal-line drive circuit for driving the signal lines, and the scanning-line drive circuit for driving the scanning lines. In this case, those drive circuits may be so designed as to be connected with one threshold value control circuit, to thereby commonly control the threshold values of the respective thin-film transistors, or the respective drive circuits may be so designed as to be connected with individual threshold value control circuits, to thereby control the threshold values of the respective thin-film transistors, independently. In particular, in the latter case, the threshold values of the respective thin-film transistors can be controlled by the first threshold value control circuit so as to improve the operating frequency of the signal-line drive circuit, and also they can be controlled by the second threshold value control circuit so as to reduce the power consumption of the scanning-line drive circuit. The reason why the threshold values are controlled independently is that the signal-line drive circuit and the scanning-line drive circuit are different in operating frequency. In other words, the operating frequency is more important to the signal-line drive circuit, whereas the power consumption is more important to the scanning-line drive circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be more fully understood from the detailed description given hereinbelow and the accompanying drawings which are given by way of illustration only, and thus are not limitative of the present invention, and wherein:

FIG. **1** is a diagram showing a matrix type liquid-crystal display unit in accordance with a first embodiment of the present invention;

FIG. **2** is a diagram showing an example of an active matrix using TFTs;

FIGS. **3A** and **3B** are diagrams showing a conventional example of the active matrix using amorphous silicon TFTs;

FIGS. **4A** and **4B** are diagrams showing a conventional example of the active matrix using polysilicon TFTs;

FIGS. **5A** and **5B** are graphs representative of the drain current to gate voltage characteristic of the conventional TFT;

FIG. **6** is a diagram showing an example of an invertor circuit;

FIG. **7** is a plan view showing a TFT used in the present invention;

FIGS. **8A** to **8C** are graphs representative of the drain current to gate voltage characteristic of the TFT;

FIG. **9** is a cross-sectional view showing the TFT;

FIG. **10** is a diagram showing an example of the invertor circuit;

FIGS. **11A** and **11B** show threshold value control circuits in accordance with a first embodiment of the present invention;

FIG. **12** is a diagram showing a matrix type liquid-crystal display unit in accordance with a second embodiment of the present invention;

FIG. **13** is a diagram showing a threshold value control circuit in accordance with the second embodiment of the present invention; and

FIG. **14** is a diagram showing an equivalent circuit example of the threshold value control circuit.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Now, a description will be given of the preferred embodiments of the present invention with reference to the accompanying drawings.

First, a TFT used in the present invention will be described with reference to FIG. **7**. In this embodiment, it is

assumed that the TFT is of the n-type. FIG. **7** is a structural view (a plan view) showing the n-type TFT. First, an island-like region **701** made of intrinsic polysilicon is formed. Then, a gate insulating film is formed, and a gate electrode film is formed on the gate insulating film. The gate electrode film is etched to form a gate electrode **702**. Thereafter, the island-like region **701** is doped with n-type impurities to form an n-type source/drain region **703**. In this process, no impurities are inserted immediately under the gate electrode **702** because doping is conducted after the formation of the gate electrode **702**.

Subsequently, the island-like region **701** is doped with p-type impurities to form a channel contact region **704**. In this embodiment, the island-like region **701** is doped with p-type impurities after being doped with the n-type impurities, however, the processing order may be reversed. Thereafter, an interlayer film is formed thereon to define contact holes **705**, **706** and **707**. Then, an electrode metal film is formed thereon to form a source electrode **708**, a drain electrode **709** and a threshold value control terminal electrode **710**. In this embodiment, a TFT having a threshold value control terminal can be formed. In the above processes, there is no newly added process because of CMOS so that the element can be formed in the same process as the conventional process.

Subsequently, the electric characteristic of the TFT will be described. First, the characteristic of the TFT when no voltage is applied to the threshold value control terminal electrode **710** is shown in FIG. **8**A. In this case, the characteristic of the TFT is identical with that of the conventional TFT having no threshold value control terminal electrode **710**. Then, the characteristic of the TFT when a positive voltage is applied to the threshold value control terminal electrode **710** is shown in FIG. **8**B, and the characteristic of the TFT when a negative voltage is applied thereto is shown in FIG. **8**C.

The operation of the TFT will be described with reference to a cross-sectional view of the TFT (FIG. **9**). The cross-sectional view of FIG. **9** is a cross-section taken along a dotted line A–A' of FIG. **7**. When the n-type TFT turns on, an n-type channel **905** is formed under a gate oxide film **902**. In this situation, a p-type layer **906** is formed on the lower side of the channel which is made of polysilicon. In this situation, in the floating state where no voltage is applied to the p-type layer **906**, the operation of the TFT is identical with that of the conventional TFT. However, upon applying a voltage to the channel contact region **704** from the control terminal **710**, the p-type layer **906** acts as a back gate, thereby influencing the channel **905**.

When a negative voltage is applied to the p-type layer **906**, a depletion layer **907** defined between the channel **905** which is an n-type layer of the channel and the p-type layer **906** formed under the channel **905** spreads and serves to suppress the channel **905**, thereby making it difficult to allow a current to flow into the channel **905**. As a result, the threshold value becomes large. On the other hand, when a positive voltage is applied to the p-type layer **906**, the depletion layer **907** is narrowed to make the current readily flow thereinto. As a result, the threshold value is reduced. Thus, a description was given of the n-type TFT. The same description is applied to the p-type TFT with the reverse of the polarity.

Subsequently, the operation of the drive circuit in accordance with the present invention will be described in view of the characteristic of the TFT. FIG. **10** shows an invertor array as one example of the drive circuit. This shows the invertor as an example, but the same description is applicable to a shift register, decoder or the like instead of the invertor. A CMOS invertor circuit normally includes four terminals for an input, an output, a power supply and GND. However, the invertor of the present invention includes six terminals with the addition of control terminals of the n-type TFT and the p-type TFT, and those control terminals are so controlled as to control the threshold values of the TFTs that constitutes the circuit.

FIG. **1** shows a first embodiment of the present invention. In this embodiment, a threshold value control terminal (reference numeral **710** in FIG. **7**) of the TFT that constitutes the signal-line drive circuit **101** and the scanning-line drive circuit **102** is taken out and controlled by a threshold value control circuit **103**. As described above, in the case where an attempt is made to reduce the power consumption with the TFT being in a normally on-state, a voltage lower than the GND potential is applied to the threshold value control terminal of the n-type TFT whereas a voltage higher than a supply voltage is applied to the threshold value control terminal of the p-type TFT, thus increasing the threshold value. Reference numeral **100** denotes a pixel matrix.

Also, in the case where an attempt is made to make the operating frequency of the drive circuits (**101**, **102**) high, a voltage higher than the GND potential is applied to the threshold value control terminal of the n-type TFT whereas a voltage lower than the supply voltage is applied to the threshold value control terminal of the p-type TFT, thus lowering the threshold value. In any case, the operation principle of the scanning-line drive circuit **102** and the signal-line drive circuit **101** are identical with those in the conventional case.

What is shown in FIGS. **11**A and **11**B is an example of the circuit diagram of the threshold value control circuit **103**. In this embodiment, since the control voltage is not changed with time, a p-type TFT threshold value control terminal **1104** and an n-type TFT threshold value control terminal **1105** may be connected with a voltage source **1101**, respectively, to give a required voltage thereto (FIG. **11**A), or may be connected with a variable resistor **1102** to give a voltage thereto (FIG. **11**B). In this example, in the case of controlling the threshold value, while monitoring a current value of the drive circuit or a current value of the individual TFTs, a voltage is set for optimization.

FIG. **12** shows a second embodiment of the present invention. In this example, control is conducted without making common the threshold value control voltage of the signal-line drive circuit **1201** and the scanning-line drive circuit **1202**, which is different from the first embodiment. In general, the operating frequency of the signal-line drive circuit **1201** is MHz in unit whereas that of the scanning-line drive circuit **1202** is KHz in unit. Hence, the operating frequency of the signal-line drive circuit **1201** is required to be increased whereas that of the scanning-line drive circuit **1202** is not required to be increased. Consequently, in the case of controlling the threshold value, the operating frequency is important to the signal-line drive circuit **1201**, whereas the power consumption is important to the scanning-line drive circuit **1202**. In this example, the structure of the threshold value control circuit per se is identical with that in the first embodiment. However, this embodiment is different from the first embodiment in that this embodiment uses two independent threshold value control circuits **1203** and **1204**. It should be noted that reference numeral **1200** denotes a pixel matrix.

FIG. **13** shows an example of the circuit structure of the second threshold value control circuit used in the present

invention. In this example, the threshold value control circuit is made up of not an external variable resistor or a variable voltage source but a thin-film transistor formed on a substrate which is commonly used as that of the drive circuit. In this example, the circuit is made up of a monitor TFT **1301** which is a reference of control, a load **1302** that converts a current flowing in the monitor TFT **1301** into a voltage, and an amplifier **1304** that amplifies a voltage developed across the load **1302** to apply a voltage to the threshold value control terminals of the drive circuit and the monitor TFT **1301**.

Hereinafter, the operation of the above second threshold value control circuit will be described. When the TFT **1301** is normally on, a drain current flows in the monitor TFT **1301**, thereby making a voltage develop across the load **1302**. That voltage is inputted to a non-inverse input terminal of differential inputs of the amplifier **1304** so that a differential voltage between the voltage across the load **1302** and a reference voltage **1303** is amplified and outputted. Because the differential voltage output thus amplified is adapted to the non-inverse input, it is outputted with a lowered value. The output terminal of the amplifier **1304** is connected to the voltage control terminals of the monitor TFT **1301** and the drive circuit, and in order to lower the voltage, a voltage across the threshold value control terminal is lowered, the threshold value of the TFT is increased so that the drain current flowing in the TFT is restrained. In this manner, a negative feedback is conducted in combination with the monitor TFT **1301** and the amplifier **1304**, thereby being capable of automatically controlling the threshold value.

As described above, the feedback circuit is structured assuming that the TFT is normally on. However, if the gate voltage of the monitor TFT **1301** is fixed to a potential which is not a source potential, and a reference voltage is set appropriately, the threshold value can be freely set.

What is shown in FIG. **14** is a specified example of the threshold value control circuit shown in FIG. **13** using TFTs. The amplifier is formed of an operational amplifier including a differential circuit made up of the n-type TFT and an active load made up of the p-type TFT.

In the above-mentioned embodiments, the threshold value of the TFT that forms a drive circuit is controlled. Instead, the threshold value of the TFT that forms the pixel portion may be controlled.

According to the present invention, the threshold value of the TFT is controlled by the application of a voltage, thereby being capable of reducing the power consumption of the drive circuit. Also, the operating frequency of the drive circuit is improved.

The foregoing description of a preferred embodiment of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and modifications and variations are possible in light of the above teachings or may be acquired from practice of the invention. The embodiment was chosen and described in order to explain the principles of the invention and its practical application to enable one skilled in the art to utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto, and their equivalents.

What is claimed is:

1. An active matrix type display device comprising:

a plurality of signal lines and a plurality of scanning lines vertical to said signal lines formed over a substrate;

a signal line drive circuit comprising at least one transistor, connected to said signal lines; and

a threshold value control circuit for controlling a threshold value of said transistor,

wherein said transistor comprises a source region and a drain region doped with a first conductive type impurity and a region doped with a second conductive type impurity, said first conductive type being opposite to said second conductive type,

wherein said threshold value control circuit is connected to said region doped with the second conductive type impurity through a terminal in order to increase an operating frequency of said signal line drive circuit by applying voltage to said terminal.

2. An active matrix display device according to claim **1** wherein said signal line drive circuit comprises at least one selected from an invertor, a shift register and a decoder.

3. An active matrix type display device comprising:

a plurality of signal lines and a plurality of scanning lines vertical to said signal lines formed over a substrate;

a signal line drive circuit comprising a plurality of first transistors, connected to said signal lines;

a scanning line drive circuit comprising a plurality of second transistors, connected to said scanning lines;

a first threshold value control circuit for controlling a threshold value of at least one of said first transistors; and

a second threshold value control circuit for controlling a threshold value of at least one of said second transistors,

wherein said at least one of said first transistors comprises a source region and a drain region doped with a first conductive type impurity and a region doped with a second conductive type impurity, said first conductive type being opposite to said second conductive type,

wherein said first threshold value control circuit is connected to said region doped with the second conductive type impunity through a terminal in order to increase an operating frequency of said signal line drive circuit by applying voltage to said terminal.

4. An active matrix type display device according to claim **3** wherein said signal line drive circuit comprises at least one selected from an invertor, a shift register and a decoder.

5. An active matrix type display device comprising:

a plurality of signal lines and a plurality of scanning lines vertical to said signal lines formed in a pixel portion;

a signal line drive circuit comprising a plurality of transistors, connected to said signal lines; and

a threshold value control circuit for controlling a threshold value of each at least one of said transistors and increasing an operating frequency of said signal line drive circuit.

6. An active matrix type display device according to claim **5** wherein said signal line drive circuit comprises at least one selected from an invertor, a shift register and a decoder.

7. An active matrix type display device comprising:

a plurality of signal lines and a plurality of scanning lines vertical to said signal lines formed in a pixel portion;

a signal line drive circuit comprising a plurality of first transistors, connected to said signal lines;

a scanning line drive circuit comprising a plurality of second transistors, connected to said scanning lines;

a first threshold value control circuit for controlling a threshold value of at least one of said first transistors; and

a second threshold value control circuit for controlling a threshold value of at least one of said second transistors.

8. An active matrix type display device according to claim 7 wherein said signal line drive circuit comprises at least one selected from an invertor, a shift register and a decoder.

9. An active matrix type display device comprising:

a plurality of signal lines and a plurality of scanning lines vertical to said signal lines formed over a substrate;

a signal drive circuit comprising a plurality of transistors, connected to said signal lines; and

a threshold value control circuit for controlling a threshold value of at least one of said transistors,

wherein said at least one of said transistors comprises a source region and a drain region doped with a first conductive type impurity and a region doped with a second conductive type impurity, said first conductive type being opposite to said conductive type,

wherein said threshold value control circuit is connected to said region doped with the second conductive type impunity through a terminal.

10. An active matrix type display device according to claim 9 wherein said signal line drive circuit comprises at least one selected from an invertor, a shift register and a decoder.

11. An active matrix type display device comprising:

a plurality of signal lines and a plurality of scanning lines vertical to said signal lines formed over a substrate;

a signal line drive circuit comprising a plurality of first transistors, connected to said signal lines;

a scanning line drive circuit comprising a plurality of second transistors, connected to said scanning lines;

a first threshold value control circuit for controlling a threshold value of at least one of said first transistors; and

a second threshold value control circuit for controlling a threshold value of at least one of said second transistors,

wherein each said at least one of said first transistors comprises a source region and a drain region doped with a first conductive type impurity and a region doped with a second conductive type impurity, said first conductive type being opposite to said second conductive type,

wherein said first threshold value control circuit is connected to said region doped with the second conductive type impurity through a terminal.

12. An active matrix type display device according to claim 11 wherein said signal line drive circuit comprises at least one selected from an invertor, a shift register and a decoder.

13. An active matrix type display device comprising:

a plurality of signal lines a plurality of scanning lines vertical to said signal lines formed in a pixel portion;

a signal line drive circuit comprising a plurality of transistors, connected to said signal lines; and

a threshold value control circuit for decreasing a threshold value of each of said transistors and increasing an operating frequency of said signal line drive circuit,

wherein said signal line drive circuit comprises at least one selected from an invertor, a shift register and a decoder.

14. An active matrix type display device comprising:

a plurality of signal lines and a plurality of scanning lines vertical to said signal lines formed in a pixel portion;

a signal line drive circuit comprising a plurality of first transistors, connected to said signal lines;

a scanning line drive circuit comprising a plurality of second transistors, connected to said scanning lines;

a first threshold value control circuit for decreasing a threshold value of at least one of said first transistors and increasing an operating frequency of said signal line drive circuit; and

a second threshold value control circuit for controlling a threshold value of at least one of said second transistors.

15. An active matrix type display device according to claim 14 wherein said signal line drive circuit comprises at least one selected from an invertor, a shift register and a decoder.

* * * * *

APPENDIX E

***Black* Reference**

U.S. Patent No. 6,412,977

US006412977B1

(12) **United States Patent**
Black et al.

(10) **Patent No.: US 6,412,977 B1**
(45) **Date of Patent: Jul. 2, 2002**

(54) **METHOD FOR MEASURING TEMPERATURE WITH AN INTEGRATED CIRCUIT DEVICE**

(75) Inventors: **Donald Lee Black**, Erie, CO (US); **Robert Walter Brown**, Medina, OH (US); **Richard Stephen Pollack**; **Dale Lee Yones**, both of Boulder, CO (US)

(73) Assignee: **The Goodyear Tire & Rubber Company**, Akron, OH (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/622,680**

(22) PCT Filed: **Apr. 14, 1998**

(86) PCT No.: **PCT/US98/07575**

§ 371 (c)(1),
(2), (4) Date: **Aug. 18, 2000**

(87) PCT Pub. No.: **WO99/53279**

PCT Pub. Date: **Oct. 21, 1999**

(51) **Int. Cl.**[7] **G01K 7/00**; G01K 7/01; G05F 1/00

(52) **U.S. Cl.** **374/178**; 323/315; 327/539; 327/538; 327/543

(58) **Field of Search** 374/141, 153, 374/178; 327/538, 543, 539, 512; 323/315

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Primary Examiner—Diego Gutierrez
Assistant Examiner—Gail Verbitsky
(74) *Attorney, Agent, or Firm*—Howard M. Cohn

(57) **ABSTRACT**

A temperature-sensor is implemented with a temperature-sensitive component of an IC chip which functions as a radio frequency transponder capable of measuring parameters associated with an object and transmitting data to an external reader/interrogator. In use with a pneumatic tire, the transponder measures temperature and pressure within the tire. The transponder includes circuitry for controlling windows of time during which real-time temperature and pressure measurements are made, and for storing calibration data, transponder ID number and the like, and for transmitting this information in a data stream to the reader/interrogator. An excessive temperature condition may also be sensed and included in the data stream.

2 Claims, 5 Drawing Sheets

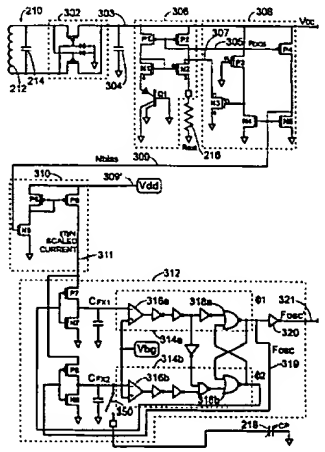

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Figure 1
Prior Art

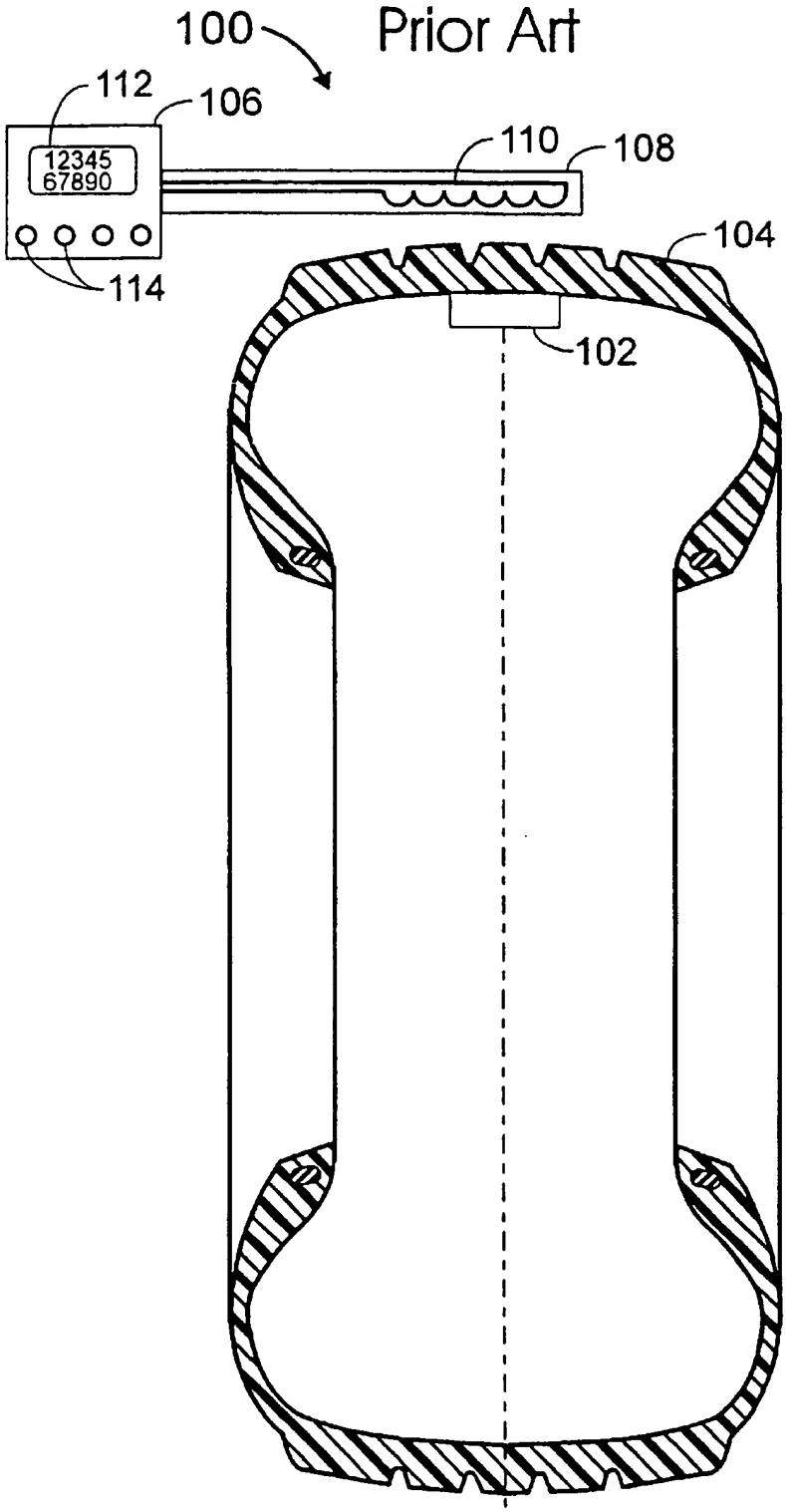
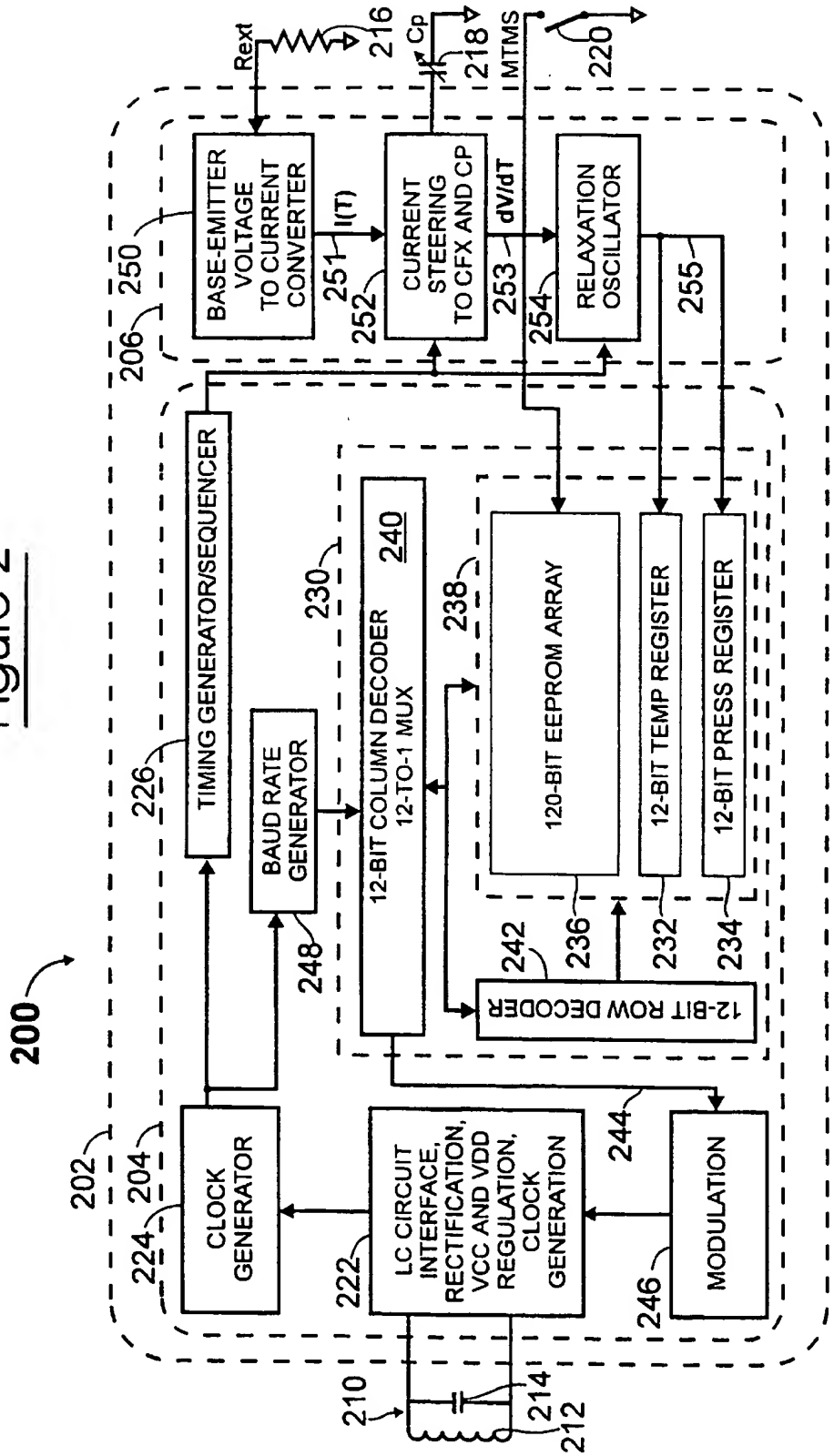


Figure 2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246
248
250
251
252
253
254
255
Rext
Cp
MTMS
I(T)
dV/dT
BASE-EMITTER VOLTAGE TO CURRENT CONVERTER
CURRENT STEERING TO CFX AND CP
RELAXATION OSCILLATOR
TIMING GENERATOR/SEQUENCER
BAUD RATE GENERATOR
12-BIT COLUMN DECODER 12-TO-1 MUX
120-BIT EEPROM ARRAY
12-BIT TEMP REGISTER
12-BIT PRESS REGISTER
12-BIT ROW DECODER
CLOCK GENERATOR
LC CIRCUIT INTERFACE, RECTIFICATION, VCC AND VDD REGULATION, CLOCK GENERATION
MODULATION

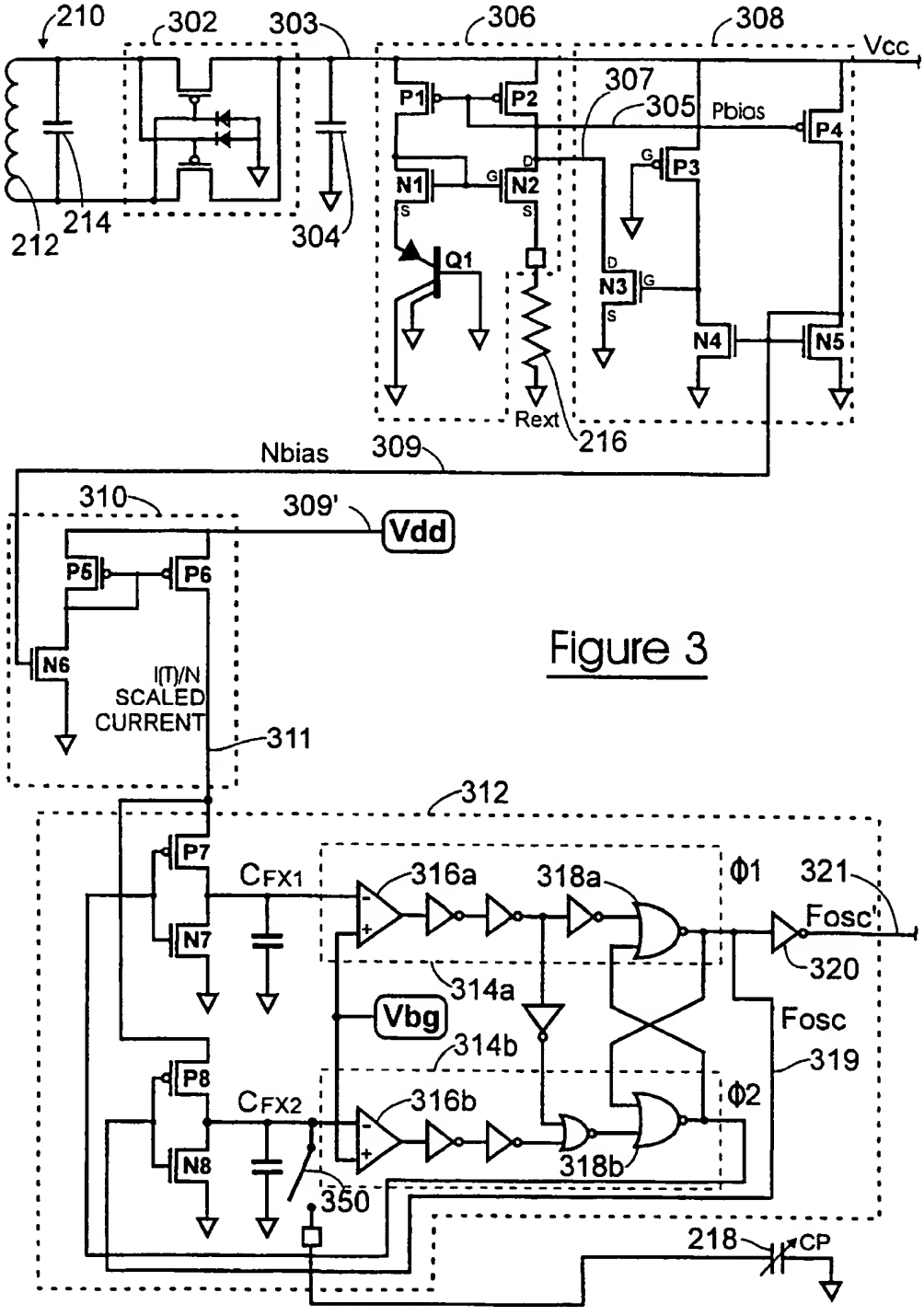

210
302
303
306
308
Vcc
307
305
Pbias
P1
P2
P3
P4
N1
N2
N3
N4
N5
Q1
Rext
216
212
214
304
Nbias
309
310
309'
Vdd
P5
P6
N6
I(T)/N
SCALED
CURRENT
311
312
P7
N7
CFX1
316a
318a
Φ1
321
Fosc'
320
314a
Vbg
314b
Fosc
319
P8
N8
CFX2
316b
Φ2
318b
350
218
CP

Figure 3

Figure 3A

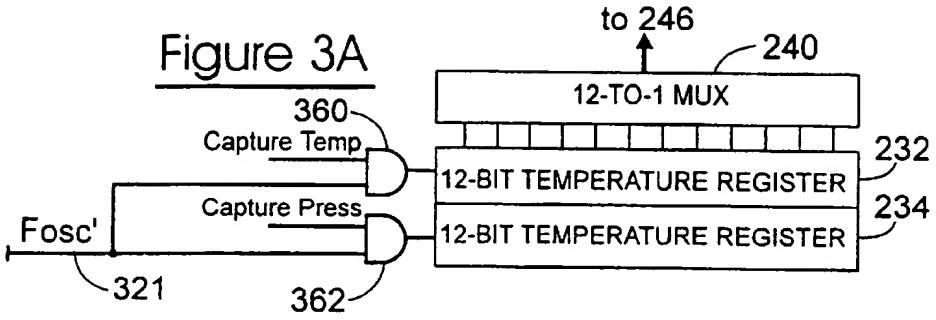


Figure 3B

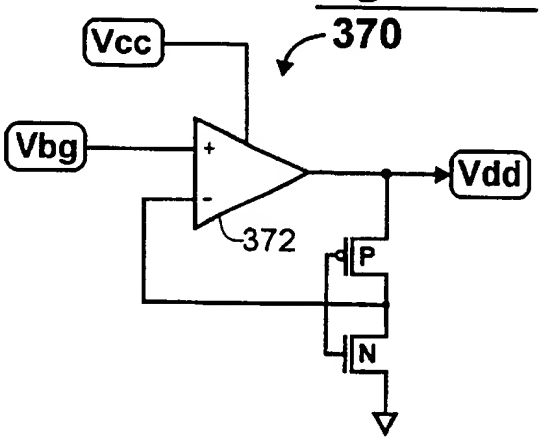
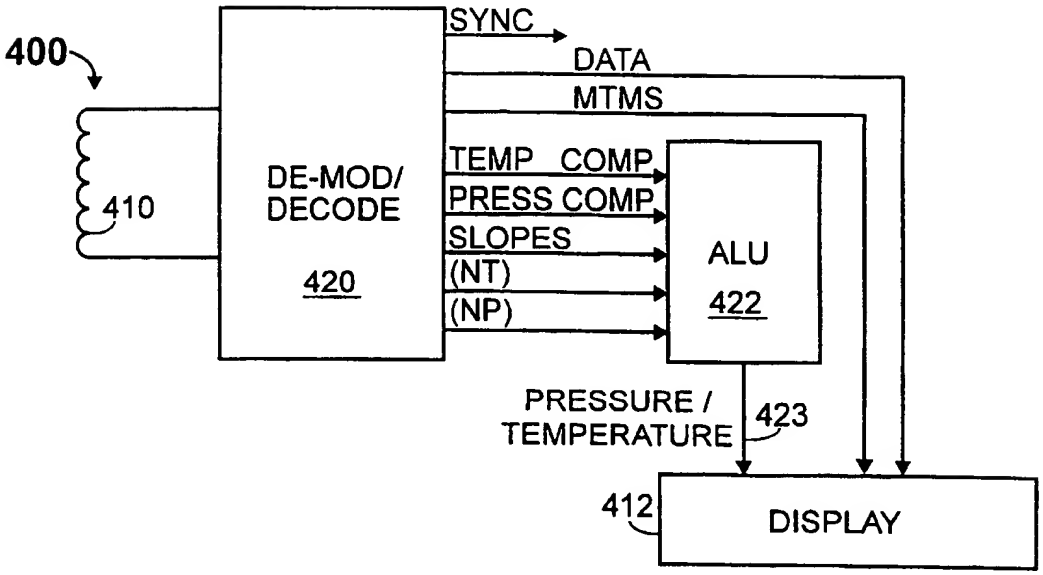


Figure 3C

←12 COLUMNS→	
ROW 1	SYNC 000..011
ROW 2	DATA 012..023
ROW 3	DATA 024..035
ROW 4	DATA 036..047
ROW 5	DATA 048..059
ROW 6	DATA 060..071
ROW 7	DATA 072..082, MTMS 083
ROW 8	TEMP COMP 084..095
ROW 9	PRESS COMP 096..107
ROW 10	TEMP/PRESS SLOPES 108..113, 114..119
ROW 11	TEMP COUNT (NT) 120..131
ROW 12	PRESS COUNT (NP) 132..143

Figure 4


400
410
DE-MOD/
DECODE
420
SYNC
DATA
MTMS
TEMP COMP
PRESS COMP
SLOPES
(NT)
(NP)
ALU
422
PRESSURE /
TEMPERATURE
423
412
DISPLAY

METHOD FOR MEASURING TEMPERATURE WITH AN INTEGRATED CIRCUIT DEVICE

TECHNICAL FIELD OF THE INVENTION

The present invention relates to the measurement of temperature and, more particularly, to measuring temperature with a device that is incorporated into an integrated circuit (IC) chip having additional (i.e. other than temperature-sensing) functionality.

BACKGROUND OF THE INVENTION

A first type of temperature-sensing device is capable of outputting a state signal indicative of whether a sensed temperature is either above or below a predetermined threshold temperature. A household thermostat is exemplary of such a threshold-sensing device. A second type of temperature-sensing device is capable of sensing temperature across a range of temperatures, and outputting a signal which varies in magnitude in proportion to the measured temperature. An electronic clinical thermometer is exemplary of such a temperature-sensing device.

The present invention is directed to the type of temperature-sensing device which is capable of outputting a signal which varies in magnitude in proportion to a sensed temperature, such a device being referred to hereinafter as a "temperature-measuring" device.

The present invention is further directed to sensing temperature with a temperature-measuring device which is implemented on an integrated circuit (IC) chip, the IC chip having intended functionality other than temperature measurement.

U.S. Pat. No. 5,039,878 (August 1977), incorporated in its entirety by reference herein, discloses a temperature sensing circuit. A semiconductor junction device (D1) integrated on an integrated circuit (IC) chip is used to generate a first signal (V1) having a known variation with temperature. A second signal (V2) is generated by passing a current (I2) which is proportional to absolute temperature through a resistor (R1), and also has a known variation with temperature which is opposite in sign to that of the first signal (V1). The two signals are compared to generate an output signal which is dependent on whether the temperature of the chip is below or above a predetermined threshold temperature. In this implementation of a temperature sensing circuit, the junction device (D1) is explicitly and advertently relieved of the temperature-detecting function (see column 1, lines 55–56).

The aforementioned U.S. Pat. No. 5,039,878 is representative of a temperature-sensing application wherein it is desired to sense the temperature of an operating IC chip, it being generally well-known that heat generated (dissipated) by the operation of electronic components is a source of concern and difficulty in many electronic systems, especially in those operating in enclosed, unventilated spaces, as well as those in high-performance miniaturized systems. The mechanisms of heat-generation in electronic systems are well known and understood. In essence, any process (e.g., an operating electronic system) which consumes power generates heat. In the case of an electronic circuit, the components of the circuit heat up, which, in turn, heats up anything in contact with them, including the surrounding air.

Other prior art applications for temperature-sensing devices include: controlling or stabilizing the operating temperature of circuit elements, the precision of which is affected either by ambient temperature changes or temperature changes caused by current flow in the circuit element itself; and controlling a supply of energy to other (than the temperature-sensing) circuit elements to prevent their breakdown due to excessive temperature rise (e.g., overheating).

Reference is made to the following U.S. Patents, each of which is incorporated in its entirety herein: U.S. Pat. Nos. 3,703,651; 4,044,371; 4,854,731; 4,952,865; 4,970,497; 5,063,307; 5,213,416; 5,396,120; 5,639,163; and 5,686,858.

As mentioned hereinabove, the present invention is directed to method and apparatus for measuring temperature over a range of temperatures. Although preferably implemented on-chip, the purpose is not to regulate the operation of the IC chip itself, but rather to monitor an ambient temperature in the vicinity of the IC chip, such as the temperature within a pneumatic tire. In the main hereinafter, method and apparatus for sensing ambient temperature with a transponder associated with the pneumatic tire is discussed.

Transponder or transceiver type identification systems are well known, and generally are capable of receiving an incoming interrogation signal and responding thereto by generating and transmitting an outgoing responsive signal. The outgoing responsive signal, in turn, is modulated or otherwise encoded so as to uniquely identify or label the particular object to which the transponder element is affixed. An example of such a transponder type identification system is disclosed in U.S. Pat. No. 4,857,893, issued Aug. 15, 1989 to Carroll and incorporated in its entirety herein. This patent describes a transponder device which receives a carrier signal from an interrogator unit. This carrier signal, of frequency F, is rectified by a rectifying circuit in order to generate operating power. Alternatively, the addition of a hybrid battery allows device to be converted into a self-powered beacon device. Logic/timing circuits derive a clock signal and second carrier signal of frequency F/n from the received carrier signal. A uniquely-identifying data word is stored in a Programmable Read-Only Memory (PROM). The data word is encoded and mixed with the carrier signal in a balanced modulator circuit, the output of which is transmitted to the interrogator unit where it is decoded and used as an identifying signal. All electrical circuits of the transponder device are realized on the same monolithic semiconductor chip which may be implemented as a Complementary Metal Oxide Semiconductor (CMOS) device.

In the manufacture of pneumatic tires, it is desirable to uniquely identify each tire as soon as possible during the course of its fabrication. This is generally done by assigning an identification (ID) number to each tire. The ability to uniquely identify tires throughout their manufacture is particularly valuable in quality control in order that the source of manufacturing problems can readily be ascertained. For example, statistical process control and other methods can be used with tire identification to detect process parameters that are going out of specification to detect machinery wear, failure, or maladjustment. The identification information should be easily discernible throughout the manufacturing process, including throughout post-manufacturing (e.g., inventory control) stages.

It is also beneficial to be able to uniquely identify a tire throughout its service life (use), for example for warranty determination, and retreading of the tire should not adversely affect the ability to identify the tire. It is also important that the tire identification be readily discernible when the tire is mounted on a steel or aluminum rim (as is

normally the case), including when the rim is one of a pair of rims in a dual wheel assembly (as is common with tractor trailers).

Aside from being able to uniquely identify a tire at various stages in its manufacture and service life, it is beneficial to be able to monitor tire pressure when the tire is in use. As is known, proper tire inflation is important to proper tire performance, including road-handling, wear, and the like.

U.S. Pat. No. 4,578,992 issued Apr. 1, 1986 to Galasko, et al. and incorporated in its entirety herein, discloses a tire pressure indicating device including a coil and a pressure-sensitive capacitor forming a passive oscillatory circuit having a natural resonant frequency which varies with tire pressure due to changes caused to the capacitance value of the capacitor. The circuit is energized by pulses supplied by a coil positioned outside the tire and secured to the vehicle, and the natural frequency of the passive oscillatory circuit is detected. The natural frequency of the coil/capacitor circuit is indicative of the pressure on the pressure-sensitive capacitor.

The use of radio frequency (RF) transponders, located either within the tire or on a rim for the tire, in conjunction with electronic circuitry for transmitting a RF signal carrying tire inflation (pressure) data, is also well known.

An example of a RF transponder suitable to be installed in the carcass of a pneumatic vehicle tire is disclosed in U.S. Pat. No. 5,451,959 issued Sep. 19, 1995 to Schuermann and incorporated in its entirety herein. This patent describes a transponder system comprising an interrogation unit for communicating with a plurality of responder units. The responder unit contains a parallel resonant circuit having a coil and a capacitor for reception of a RF interrogation pulse. Connected to the parallel resonant circuit is a capacitor serving as an energy accumulator. A processor may be provided for receiving input signals from a sensor which responds to physical parameters in the environment of the responder unit 12, for example to the ambient temperature, the ambient pressure or the like. The sensor could for example be an air-pressure sensitive sensor. In this case the responder unit can be installed in the carcass of a vehicle pneumatic tire and, with the aid of an interrogation unit contained in the vehicle, it is possible to continuously monitor the air pressure in the tire.

Another example of a RF transponder suitable to be installed in the a pneumatic vehicle tire is disclosed in U.S. Pat. No. 5,581,023 issued Dec. 3, 1996 to Handfield, et al., and incorporated in its entirety herein. This patent describes a transponder and a receiving unit, preferably one transponder for each vehicle tire, and the transponder may be entirely disposed within the vehicle tire. The transponder includes a pressure sensor, and may include various other sensors such as a temperature sensor. An Application-Specific Integrated Circuit (ASIC) embodiment of the transponder is described with reference to FIG. 9 of the patent, the ASIC (300) includes an oscillator (322) controlled by an external crystal (325), a constant current device (310) providing current flowing through an external variable-resistance pressure sensor (327), a window comparator circuit (324) having a lower threshold for reporting pressure information established by external resistors (329 and 331) connected in a voltage-divider arrangement, and an upper threshold controlled by an external variable resistor (333). A number of three-position jumpers (328) are utilized to program a unique transponder unit serial number during its manufacture. The ASIC (300) is powered by an external battery (318), and a transmitting circuit (312) is external to the ASIC (300).

Another example of a RF transponder suitable to be installed in a pneumatic vehicle tire is disclosed in U.S. Pat. No. 5,661,651 issued Aug. 26, 1997 to Geschke, et al. and incorporated in its entirety herein. This patent describes a wireless system for monitoring vehicle parameters, such as tire pressure. RF signals transmitted from different tires may be distinguished based upon the frequency of the transmitted signal. In order to sense the pressure inside a tire, tire pressure monitoring systems utilize a pressure sensor located within the tire. FIG. 2 of this patent shows the preferred structure for a parameter sensor and transmitter circuit when used to monitor the pressure inside a vehicle's tire. Parameter sensor and transmitter circuit (20) includes a pressure-to-voltage transducer (21) and a battery-powered power supply circuit (24).

The need to monitor tire pressure when the tire is in use is highlighted in the context of "run-flat" (run deflated) tires, tires which are capable of being used in a completely deflated condition. Such run-flat tires may incorporate reinforced sidewalls, mechanisms for securing the tire bead to the rim, and a non-pneumatic tire (donut) within the pneumatic tire to enable a driver to maintain control over the vehicle after a catastrophic pressure loss, and are evolving to the point where it is becoming less and less noticeable to the driver that the tire has become deflated. The broad purpose behind using run-flat tires is to enable a driver of a vehicle to continue driving on a deflated pneumatic tire for a limited distance (e.g., 50 miles, or 80 kilometers) prior to getting the tire repaired, rather than stopping on the side of the road to repair the deflated tire. Hence, it is generally desirable to provide a low-pressure warning system within in the vehicle to alert (e.g., via a light on the dashboard, or a buzzer) the driver to the loss of air in a pneumatic tire. Such warning systems are known, and do not form part of the present invention, per se.

Although the use of pressure transducers in pneumatic tires, in association with electronic circuitry for transmitting pressure data is generally well known, these pressure-data systems for tires have been plagued by difficulties inherent in the tire environment. Such difficulties include effectively and reliably coupling RF signals into and out of the tire, the rugged use the tire and electronic components are subjected to, as well as the possibility of deleterious effects on the tire from incorporation of the pressure transducer and electronics in a tire/wheel system. In the context of "passive" RF transponders which are powered by an external reader/interrogator, another problem is generating predictable and stable voltage levels within the transponder so that the circuitry within the transponder can perform to its design specification.

An example of a pneumatic tire having an integrated circuit (IC) transponder and pressure transducer is disclosed in commonly-owned U.S. Pat. No. 5,218,861, issued Jun. 15, 1993 to Brown, et. al. and incorporated in its entirety by reference herein. This patent describes an RF transponder mounted within a pneumatic tire. Upon interrogation (polling) by an external RF signal provided by a "reader", the transponder transmits tire identification and tire pressure data in digitally-coded form. The transponder is "passive" in that it is not self-powered, but rather obtains its operating power from the externally-provided RF signal. The tire has two spaced beads, each including an annular tensile member of wound or cabled steel wire. The transponder antenna is positioned adjacent one of the annular tensile members for electric or magnetic field coupling to the annular tensile member.

Another example of a pneumatic tire having an integrated circuit (IC) transponder and pressure transducer is disclosed

in commonly-owned U.S. Pat. No. 5,181,975, issued Jan. 26 1993 to Pollack, et. al. and incorporated in its entirety by reference herein. As described in this patent, in a tire that has already been manufactured, the transponder may be attached to an inner surface of the tire by means of a tire patch or other similar material or device.

Another example of an RF transponder in a pneumatic tire is disclosed in commonly-owned U.S. Pat. No. 4,911,217, issued Mar. 27, 1990 to Dunn, et. al. and incorporated in its entirety by reference herein. This patent describes the transponder having two electrodes, a first of which is positioned such that the average spacing of the first electrode's surface from one of the tire's steel reinforcing components, such as an annular tensile member in its bead or a steel-reinforced ply, is substantially less than the average spacing of the second electrode's surface from the reinforcing component. FIG. 1*a* of this patent also describes a prior-art identification system ("reader") that can be used to interrogate and power the transponder within the tire. The identification system includes a portable hand-held module having within it an exciter and associated circuitry for indicating to a user the numerical identification of the tire/transponder in response to an interrogation signal.

Typically, in an IC transponder, the IC chip and other components are mounted and/or connected to a substrate such as a printed circuit board (PCB). For example, a pressure transducer may be mounted to the PCB and wired either directly to the IC chip or indirectly to the IC chip via conductive traces on the PCB. The PCB substrate is suitably a reinforced epoxy laminate having a thickness of twenty mils, and having a glass transition temperature exceeding 175° C. (degrees Celsius). A suitable PCB material is available as "high performance" FR-4 epoxy laminate, grade 65M90, sold by Westinghouse Electric Corporation, Copper Laminates Division, 12840 Bradley Avenue, Sylmar, Calif. 91342.

There have thus been described, hereinabove, a number of RF transponders suitable for mounting within a pneumatic tire. The environment within which a tire-mounted transponder must reliably operate, including during manufacture and in use, presents numerous challenges to the successful operation of the transducer. For example, the pressure sensor used with the transponder preferably will have an operating temperature range of up to 125° C., and should be able to withstand a manufacturing temperature of approximately 177° C. For truck tire applications, the pressure sensor must have an operating pressure range of from about 50 psi (pounds per square inch) to about 120 psi (from about 345 kp (kilopascals) to about 827 kp), and should be able to withstand pressure during manufacture of the tire of up to about 400 psi (about 2758 kp). The accuracy, including the sum of all contributors to its inaccuracy, should be on the order of plus or minus 3% of full scale. Repeatability and stability of the pressure signal should fall within a specified accuracy range.

The transponder must therefore be able to operate reliably despite a wide range of pressures and temperatures. Additionally, a tire-mounted transponder must be able to withstand significant mechanical shocks such as may be encountered when a vehicle drives over a speed bump or a pothole.

Suitable pressure transducers for use with a tire-mounted transponder include:

(a) piezoelectric transducers;

(b) piezoresistive devices, such as one of those disclosed in U.S. Pat. No. 3,893,228 issued in 1975 to George, et al., and in U.S. Pat. No. 4,317,216 issued in 1982 to Gragg, Jr.;

(c) silicon capacitive pressure transducers, such as is disclosed in U.S. Pat. No. 4,701,826 issued in 1987 to Mikkor;

(d) devices formed of a variable-conductive laminate of conductance ink; and

(e) devices formed of a variable-conductance elastomeric composition.

BRIEF SUMMARY OF THE INVENTION

It is a broad object of the present invention to monitor an ambient temperature in the vicinity of an integrated circuit (IC) chip as defined in one or more of the appended claims and, as such, having the capability of being constructed to accomplish one or more of the following subsidiary objects.

It is a broad object of the invention to monitor an ambient temperature in the vicinity of an integrated circuit (IC) chip, the IC chip having functionality other than temperature-sensing, such as a radio frequency (RF) transponder ("tag") capable of transmitting data related to a monitored object and parameters associated with the object to an external reader/interrogator.

It is another object of the present invention to provide a technique for utilizing the sensed temperature data, in combination with other sensed parameter data (such as pressure data), to provide a temperature-compensated value for the other sensed parameter data.

It is a further object of the invention to provide an improved radio frequency (RF) transponder ("tag") capable of transmitting data related to a monitored object and parameters associated with the object to an external reader/interrogator.

It is another object of the present invention to provide pressure data from a transponder to an external reader/interrogator in a manner in which temperature-dependency of the pressure data can be eliminated from the pressure data, resulting in a temperature-compensated pressure measurement being displayed by the external reader/interrogator.

According to the invention, a predictable temperature-dependent characteristic voltage of a temperature-sensitive component of an integrated circuit (IC) chip, for example the base-emitter voltage (Vbe) of a lateral bipolar transistor (Q1), is superimposed across an external precision resistor (Rext). A temperature-dependent current I(T) is thereby caused to flow through the external resistor (Rext). The temperature-dependent current flowing though the external resistor is provided (e.g., mirrored) to another circuit on the IC chip, the output of which is proportional to the temperature-dependent current I(T) flowing through the resistor. In an embodiment of the invention, the other circuit is a relaxation oscillator, and the output of the other circuit is a temperature-dependent frequency. Inasmuch as the temperature sensor is preferably implemented "on-chip" it should be understood that the IC chip should be a low-power device that generates relatively little internal heat, as contrasted with ambient heat being sensed by the on-chip temperature sensor.

According to an aspect of the invention, the IC chip functions as a radio-frequency (RF) transponder comprising circuitry capable of transmitting information unique to an object with which the transponder is associated to an external reader/interrogator. The temperature-sensitive component (temperature sensor), and one or more additional sensors (transducers) provide real-time parameter measurement at the transducer location. These measurements are trans-

mitted to the external reader/interrogator, in the form of data, in a data stream on a signal which is output by the transponder, such as by impressing (modulating) the data stream onto a RF signal transmitted by the transponder to the external reader/interrogator.

According to an aspect of the invention, the transponder is preferably powered by an RF signal from the external reader/interrogator. However, it is within the scope of this invention that the transponder is battery-powered.

According to an aspect of the invention, the transponder is preferably implemented on a single integrated circuit (IC) chip, with a minimum of external instrumentalities such as an antenna.

According to an aspect of the invention, at least one real-time parameter which is measured is temperature. Preferably, the temperature sensor is embedded ("on-chip") in the IC chip of the transponder.

According to an aspect of the invention, an additional real-time parameter which may be measured is pressure. Pressure is preferably measured by a separate ("off-chip") pressure sensor, which is preferably of a type that varies its capacitance value as a function of ambient pressure. Preferably, the temperature sensor is disposed so as to be subject to substantially the same ambient temperature as the pressure sensor so that a true, temperature-compensated pressure can readily be calculated.

According to an aspect of the invention, another additional parameter which may be measured is in the form of an indication that an excessively high temperature condition, albeit transient, has previously occurred. It should be understood that this parameter is different in nature than the real-time parameters of temperature and pressure. An example of a sensor suitable for sensing and indicating that such a transient over-temperature condition has occurred can be found in U.S. Pat. No. 5,712, 609, issued Jan. 27, 1998 to Mehregany, et al. and incorporated by reference in its entirety herein. Mehregany's sensor is cited as being exemplary of a suitable Maximum Temperature Measurement Switch (MTMS) for use with the transponder of the present invention. Reference is also made to U.S. Pat. No. 5,706,565 which is incorporated in its entirety by reference herein.

The transponder is primarily intended to be associated with a pneumatic tire, and is preferably located within the tire. However, it is within the scope of this invention that the transponder is associated with another object being monitored, such as an animal.

In a preferred embodiment, the transponder comprises:

- circuitry for receiving an RF signal at a first frequency (Fi) from the external reader/interrogator and processing the received RF signal to provide power and clock pulses to other circuitry;
- circuitry for controlling window(s) of time during which real-time parameter measurement(s) is (are) made, and captured;
- circuitry for storing calibration constants; and
- circuitry for impressing (preferably by Phase Shift Keying (PSK) modulation) the captured real-time parameter measurements and excessive temperature condition indication onto a signal which is transmitted back to the external reader/interrogator at a second frequency (Fc) which is different from the first frequency (Fi).

Other objects, features and advantages of the invention will become apparent in light of the following description thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

Reference will be made in detail to preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. The drawings are intended to be illustrative, not limiting.

Certain elements in selected ones of the drawings may be illustrated not-to-scale, for illustrative clarity.

Often, similar elements throughout the drawings may be referred to by similar reference numerals. For example, the element 199 in a figure (or embodiment) may be similar in many respects to the element 299 in another figure (or embodiment). Such a relationship, if any, between similar elements in different figures or embodiments will become apparent throughout the specification, including, if applicable, in the claims and abstract.

In some cases, similar elements may be referred to with similar numbers in a single drawing. For example, a plurality of elements 199 may be referred to as 199*a*, 199*b*, 199*c*, etc.

The cross-sectional views presented herein may be in the form of "slices", or "near-sighted" cross-sectional views, omitting certain background lines which would otherwise be visible in a true cross-sectional view, for illustrative clarity.

The structure, operation, and advantages of the present preferred embodiment of the invention will become further apparent upon consideration of the following description taken in conjunction with the accompanying drawings, wherein:

FIG. **1** is a generalized block diagram of a RF transponder system comprising an external reader/interrogator and a RF transponder within a pneumatic tire, according to the prior art;

FIG. **2** is a block diagram of major components of a RF transponder, according to the present invention;

FIG. **3** is a schematic diagram of major portions of the RF transponder of FIG. **2**, according to the present invention;

FIG. **3A** is a schematic diagram of a portion of the RF transponder of FIG. **2**, according to the invention;

FIG. **3B** is a schematic diagram of a portion of the RF transponder of FIG. **2**, according to the invention;

FIG. **3C** is a diagram of a memory space within the RF transponder of FIG. **2**, illustrating how data may be arranged and transmitted, according to the invention; and

FIG. **4** is a schematic block diagram of a receiving portion of a reader/interrogator, according to the invention.

DETAILED DESCRIPTION OF THE INVENTION

FIG. **1** illustrates a RF transponder system **100** of the prior art, comprising a RF (radio frequency) transponder **102** disposed within (e.g., mounted to an inner surface of) a pneumatic tire **104**, An antenna, not shown, is mounted within the tire **104** and is connected to the transponder **102**. The transponder **102** is an electronic device, capable of transmitting an RF signal comprising unique identification (ID) information (e.g., its own serial number, or an identifying number of the object with which it is associated—in this example, the tire **104**) as well as data indicative of a parameter measurement such as ambient pressure sensed by a sensor (not shown) associated with the transponder **102** to an external reader/interrogator **106**. The external reader/interrogator **106** provides an RF signal for interrogating the transponder **102**, and includes a wand **108** having an antenna **110**, a display panel **112** for displaying information transmitted by from the transponder **102**, and controls (switches, buttons, knobs, etc.) **114** for a user to manipulate the functions of the reader/interrogator **106**. The present invention is directed primarily to implementing the RF transpon-

der. Nevertheless, certain functionality for a reader/interrogator to be compatible with the transponder of the present invention is discussed hereinbelow with respect to FIG. **4**.

As is known, the ID and/or parameter measurement information may be encoded (impressed) in a variety of ways on the signal transmitted by the transponder **102** to the reader/interrogator **106**, and subsequently "de-coded" (retrieved) in the reader/interrogator **106** for display to the user. The RF transponder **102** may be "passive", in that it is powered by an RF signal generated by the external reader/interrogator **106** and emitted by the antenna **108**. Alternatively, the RF transponder may be "active",in that it is battery-powered. Transponder systems such as the transponder system **100** described herein are well known.

FIG. **2** is a block diagram of the RF transponder **200** (compare **102**) of the present invention, illustrating the major functional components thereof.

The transponder **200** is preferably implemented on a single integrated circuit (IC) chip shown within the dashed line **202**, to which are connected a number of external components. Other dashed lines in the figure indicate major functional "blocks" of the transponder **200**, and include a transponder "core" **204** and a sensor interface **206**. The components external to the IC chip **202** include an antenna system **210** comprising an antenna **212** and a capacitor **214** connected across the coil **212** to form an L-C resonant tank circuit, an external precision resistor ("Rext") **216**, an external pressure-sensing capacitor ("C_P") **218**, and an optional external maximum temperature measurement switch ("MTMS") **220**. The antenna may be in the form of a coil antenna, a loop antenna, a dipole antenna, and the like. Alternatively, the signal output by the transponder may be provided on a transmission line. In the main hereinafter, a transponder having a coil antenna is described.

The transponder core **204** includes interface circuitry **222** for processing an RF signal, such as a 125 kHz (kilohertz) un-modulated carrier signal received by the antenna **212**, for rectifying the received RF signal, and for providing voltages for powering other circuits on the IC chip **202**. For example, the interface circuitry provides a regulated supply voltage (Vdd) of 2.5 volts, and a temperature-independent bandgap voltage (Vbg) of 1.32 volts. The provision of various supply and reference voltages for the transponder circuitry are described in greater detail hereinbelow, with reference to FIG. **3B**. The interface circuitry **222** also provides the received RF signal, preferably at the frequency (Fi) it is received, to a clock generator circuit **224** which generates clock signals in a known manner for controlling the timing of other circuits on the IC chip **202** as well as the frequency (Fc) of a signal which is transmitted by the transponder to the external reader/interrogator.

A timing generator/sequencer circuit **226** receives the clock pulses from the clock generator circuit **224** and processes (e.g., divides) the clock pulses to generate timing windows (W_T and W_P, described hereinbelow) for predetermined periods of time during which parameter (e.g., temperature and pressure) measurements are made. The timing windows (W_T and W_P) may either be of substantially equal duration or of unequal duration. The timing generator/sequencer circuit **226** also controls the timing and sequence of various functions (e.g., pressure measurement and capture, temperature measurement and capture, described in greater detail hereinbelow) performed in the sensor interface **206**, and is preferably implemented as an algorithmic state machine (ASM).

The transponder core **204** further includes a register/counter circuit **230** which includes a temperature register **232** (e.g., 12-bit) and a pressure register **234** (e.g., 12-bit) for capturing and storing temperature and pressure measurements (counts), respectively, and a block **236** of addressable memory, which includes an EEPROM array. The registers **232** and **234** and EEPROM array **236** are shown in a dashed line **238** representing a block of addressable memory on the IC chip.

The register/counter circuit **230** also includes a multiplexer and column decoder **240**, as well as a row decoder **242** for controlling the sequence in which signals (i.e., data) are output on a line **244** to a modulation circuit **246** which, via the interface circuitry **222**, communicates selected measured tire-operating characteristics in a data stream via the antenna interface **210** to the external reader/interrogator (**106**, FIG. **1**).

The transponder core **204** also includes a baud rate generator **248** which controls the rate at which modulating information (e.g., the temperature or pressure measurement) is applied to the modulation circuit **246**. The baud rate generator **248** also provides a data carrier clock controlling the output frequency (Fc) of the transponder and a data rate clock controlling a rate at which the data stream including measurements, calibration information, etc. is modulated onto the transponder output carrier.

The sensor interface **206** includes a circuit **250** for generating an output current I(T) on a line **251** which is related to a predictable characteristic voltage of a temperature-sensitive component (e.g., Vbe of a transistor Q1, described hereinbelow) which is superimposed on the external resistor (Rext) **216**. The output current I(T) on the line **251** is provided to a current steering circuit **252** and to a relaxation oscillator **254**. In general terms, the relaxation oscillator **254** oscillates at a frequency controlled by a rate of voltage change (dV/dT) produced on an output line **253** from the current steering circuit **252**. The rate of voltage change on the line **253** is a function of the output current I(T) on line **251** and of internal capacitances (C_{FX}) associated with the relaxation oscillator as well as an external capacitance (C_P) that can be switched into the oscillator circuit. An output signal from the relaxation oscillator **254** is provided on a line **255** which, as will be explained in greater detail hereinbelow, is indicative of both ambient temperature and ambient pressure. As used herein, the term "ambient" refers to the parameter being measured in the vicinity of the transponder, more particularly the respective sensors associated with the transponder. When the transponder is mounted within a pneumatic tire, "ambient pressure" refers to the pressure within the tire.

In operation, an RF signal from an external source (i.e., reader/interrogator, not shown, compare **106**, FIG. **1**) is received by the antenna **212**. This RF signal is rectified and used to power the RF transponder **200**. Modulating information applied to the modulation circuit **236** is used to alter characteristics of the antenna interface (e.g., impedance, resonant frequency, etc.). These alterations are sensed by the external reader/interrogator and are decoded, providing communication of temperature and pressure information back from the RF transponder **200** to the external reader/interrogator.

The timing generator/sequencer circuit **226** controls whether the current I(T) on the line **251** is "steered" into one or the other of two capacitors (C_{FX1} or C_{FX2}, described hereinbelow with respect to the relaxation oscillator **312**) associated with the relaxation oscillator **254**, and whether

the external pressure-sensing capacitance (C_P) **218** is or is not included in the generation of an output signal (Fosc) by the relaxation oscillator **254**. For example, to measure temperature, the current I(T) is steered into the internal oscillator capacitors (C_{FX}), but the pressure-sensing capacitor (C_P) is disconnected from (not included in) those capacitances. This means that the frequency of the oscillator output signal seen on line **255** is a function of temperature alone. When the pressure-sensing capacitor (C_P) **218** is "switched in", then the output frequency of the oscillator **254** on the line **255** will, as explained in greater detail hereinbelow, be a function of both pressure and temperature. As described in greater detail hereinbelow, an algorithm is employed in the reader/interrogator to generate a temperature-independent measurement of pressure.

As controlled by the timing generator/sequencer circuit **226**, either the 12-bit temperature register **232** or the 12-bit pressure register **234** (depending upon whether temperature or pressure is being measured) counts (captures) oscillations of the oscillator output signal on line **255**. (Counters, not shown, are associated with these "registers.) The timing "window" provided by the timing generator/sequencer circuit **226** has a known, controlled duration. As a result, the count remaining in (captured by) the respective temperature or pressure counter (register) when the timing window "closes" is a function of (proportional to) the oscillation frequency (Fosc) of the relaxation oscillator **254**, and therefore a function of temperature or pressure, whichever is being measured.

The EEPROM array **236** is used to hold calibration constants that the reader system uses to convert temperature and pressure counts (N_T and N_P, respectively, described in greater detail hereinbelow) into temperature and pressure readings which can be displayed (e.g., via display **112**) to a user. The EEPROM array **236** can also store the ID of the transponder, calibration data for the transponder, and other data particular to the given transponder.

FIG. **3** is a more-detailed schematic diagram **300** of several of the components of the transponder **200** of FIG. **2**, primarily those components described hereinabove with respect to the sensor interface section **206** of FIG. **2**.

In this schematic diagram **300**, conventional circuit symbols are employed. For example, lines which cross over one another are not connected to one another, unless there is a "dot" at their junction (cross-over), in which case the lines are connected with one another. Conventional symbols are employed for transistors, diodes, ground connections, resistors, capacitors, switches, comparators, inverters, and logic gates (e.g., "AND", "NAND", "OR", "NOR").

The circuit is described in terms of a CMOS embodiment, wherein "P" (e.g., "P1") indicates a PMOS (P-channel) transistor and "N" (e.g., "N1") indicates an NMOS (N-channel) transistor. CMOS transistors are of the FET (field effect transistor) type, each having three "nodes" or "terminals"—namely, a "source" (S), a "drain" (D), and a "gate" (G) controlling the flow of current between the source and the drain. In the description that follows, it will be evident that a number of the PMOS and NMOS transistors are "diode-connected", meaning that their drain (D) is connected to their gate (G). The general theory of operation of transistors, particularly CMOS transistors, is well-known to those having ordinary skill in the art to which the present invention most nearly pertains.

As will evident from the description that follows, a number of the CMOS transistors are connected in a "current-mirroring" configuration. The concept of current-mirroring is well known, and in its simplest form comprises two similar polarity transistors (e.g., two PMOS transistors) having their gates connected with one another, and one of the pair of transistors being diode-connected. Current-mirroring generally involves causing a current to flow through the diode-connected transistor, which results in a gate voltage on the diode-connected transistor required to produce that current. Generally, the gate voltage of the diode-connected transistor is forced to become whatever voltage is necessary to produce the mirrored current through that transistor. Since the diode-connected transistor, by definition, has no gate current, by applying the gate voltage of the diode-connected transistor to any other identically-connected transistor, a mirrored-current will flow through the identically-connected transistor. Typically, the current-mirroring transistors all have the same physical area, in which case the mirrored current will be essentially same as the current which is being mirrored. It is also known to produce a mirrored current which is either greater than or less than the current being mirrored by making one of the transistors physically larger or smaller (in area) than the other. When such identically-connected transistors having different areas are connected in a current-mirroring configuration, their scaled (larger or smaller) areas will produce correspondingly scaled (larger or smaller) currents.

In the main hereinafter, the numerous connections between the various components of the circuit are clearly illustrated in the figure, and the descriptive emphasis is on the various functions of and interactions between the various components of the circuit rather than on reciting (ad nauseam) each and every individual connection between the various components, all of which are explicitly illustrated in the figure.

The antenna system **210** comprises a coil antenna **212** and a capacitor **214** connected across the antenna **212** to form an L-C resonant tank circuit providing an alternating current (AC) output to a full-wave rectifier circuit **302**.

The full-wave rectifier circuit **302** comprises two PMOS transistors and two diodes, connected in a conventional manner, as shown, and outputs a full wave rectified direct current (DC) voltage on a line **303**. A capacitor **304** is connected between the line **303** and ground to "smooth out" (filter) variations ("ripple") in the full wave rectified DC voltage on the line **303**. The voltage on the line **303** thus becomes a usable voltage for the remaining components of the transponder—in this case, a positive supply voltage (Vcc) on the line **303**.

A temperature-sensing circuit **306**, corresponding approximately to the base-emitter voltage-to-current converter **250** of FIG. **2**, is connected between the line **303** (Vcc) and ground, and includes four CMOS transistors labeled **P1**, **P2**, **N1** and **N2** and a lateral bipolar transistor labeled **Q1**, and is connected to the external resistor **216** (Rext). The transistors **P2** and **N1** are diode-connected, as illustrated. The two transistors **P1** and **P2** are connected in a current-mirroring configuration, and the two transistors **N1** and **N2** are also connected in what can generally be considered to be a current-mirroring configuration. The source of the transistor **N1** is connected via the transistor **Q1** to ground, and the source of the transistor **N2** is connected via a the external resistor (Rext) **216** to ground.

As will become evident, the ability of the temperature-sensing circuit **306** to produce a signal (i.e., a current) that is proportional to a sensed (ambient) temperature (e.g., within the tire with which the transponder is associated) is largely dependent on the characteristic that the base-emitter

voltage of the transistor Q1 is a highly predictable and repeatable function of temperature. The resistor (Rext) **216** is an external, precision, reference resistor, whose value is substantially independent of temperature (as contrasted with the temperature dependency of the transistor Q1). A suitable value for the resistor (Rext) **216** is 20.5 kΩ.

The transistor N2 is connected between the transistor P2 and the external resistor **216** (Rext) in a "source-follower" mode. As a voltage is impressed on the gate of the transistor N2, its source voltage will "follow" its gate voltage (minus an inherent voltage drop (Vgs) between its gate and its source).

As current flows through the transistor N1, its gate voltage will be offset by its gate-source voltage drop (Vgs) above the emitter voltage at the transistor Q1. Since the transistors N1 and N2 are essentially identical, with the same current flowing through each of the two transistors N1 and N2, they will have identical gate-source voltage drops (Vgs). As a result, the voltage at the source of the transistor N2 across the external resistor **216** (Rext) will be essentially identical to the voltage at the emitter of the transistor Q1. Hence, applying Ohm's law (E=IR, or I=E/R), the current through the external resistor **216** (Rext) will equal the emitter voltage of the transistor Q1 divided by the resistance of the external resistor **216** (Rext).

In normal operation, all of the current flowing through the external resistor (Rext) **216** flows through the source of the transistor N2 and, consequently, through the diode-connected transistor P2. By a current-mirroring connection, the current through the transistor P2 is replicated (mirrored) in the transistor P1 and is further replicated (mirrored) in the transistor P4. This ensures that the current flowing through the transistors N1 and N2 will be the same, at all times, which further helps to ensure that the emitter voltage at the transistor Q1 and the voltage across the external resistor (Rext) **216** are identical, independent of voltage and process variations. As mentioned hereinabove, the transistors N1 and N2 are connected in what can generally be considered to be a current-mirroring configuration. However, since they are not strictly identically connected, their function in the circuit **306** is principally for "matching" Q1 and Rext.

In essence, the circuit **306** ensures that the current I(T) flowing through the external resistor (Rext) is predictable, and is a function of the absolute temperature (T) of the transistor Q1. As described in greater detail hereinbelow, this temperature-dependent current I(T) flowing through the external resistor (Rext) **216** is mirrored to a relaxation oscillator (**312**, described hereinbelow) to provide a signal indicative of the temperature of the transistor Q1 to the external reader (**106**, FIG. **1**). As described in greater detail hereinbelow, the output frequency (Fosc) of the relaxation oscillator **312** will be a function of the absolute temperature (T) of the transistor Q1.

At this point, it is useful to note that it is essentially the transistor Q1 that is being employed as the temperature-sensing element of the overall transponder circuit. The transponder circuit advantageously employs an inherent characteristic of such a transistor implemented in CMOS technology that the base-emitter voltage of the transistor Q1 will vary by a predictable amount of −2.2 mv/° C. (millivolts per degree Celsius).

It should be noted that the transponder of the present invention is described in terms of a "passive" device, relying on RF energy being supplied to it by an external source (**106**, FIG. **1**) to power up its circuitry. However, it is within the scope of this invention that the transponder contain its own power supply, such as in the form of a battery. In either case, when first powering up circuitry such as described with respect to the temperature-sensing circuit **306**, it is important to ensure that they "ramp up" to their normal operating state from their quiescent state in a reliable and predictable (controlled) manner. To this end, two lines **305** and **307** are illustrated which are connected between the temperature-sensing circuit **306** and a "startup" circuit **308**.

The startup circuit **308** is connected between the supply voltage (Vcc) on the line **303** and ground, and serves two main purposes: (i) to get current flowing in the temperature-sensing circuit **306** when the transponder (**200**) first starts up from a powered down state; and (ii) to mirror and convert the current flowing through the transistor P2 from a supply-referenced current to a ground-referenced current.

Startup is initiated by the transistor P3. The transistor P3 is fabricated to have high channel resistance so as to function in a "weak pull-up" mode. With its gate connected to ground, it will always be "on", and will behave essentially like a resistor having a fairly high resistance (e.g., >10 k ohms).

Since, at startup, no current flows elsewhere in the circuit, the transistor P3 operates to pull the gate of the transistor N3 towards the supply voltage (Vcc), thereby turning the transistor N3 "on", which effectively connects the transistor's N3 source to its drain which, in turn, causes current to flow through the diode-connected transistor P2 of the temperature-sensing **306** into the drain of the transistor N3. This causes the voltage at the source of the transistor P2 to decrease, thereby causing current to flow in the transistors P1 and P4. As current flows through the transistor P4 into the diode-connected transistor N5, a current-mirroring connection between the transistors N4 and N5 causes a corresponding current to flow through the transistor N4, thereby pulling the gate of transistor N3 to ground, thereby effectively shutting "off" the flow of current through the transistor N3.

However, with current now flowing through the current-mirrored transistors P1, P2 and P4, current flowing from the transistor P1 through the transistor N1 into the transistor Q1 forces the temperature-sensing circuit **306** to "start up" in its stable operating point state (rather than its zero current state). After startup, the transistor N3 essentially "drops out" of the circuit, having performed its intended function.

The transistor N5 is connected in a current-mirroring configuration with the transistor N4 (and, as described hereinbelow, with the transistor N6). Therefore, essentially, with a current equivalent to the current through the external resistor (Rext) **216** flowing through the transistor N5, the same current flows through the transistor N4, thereby establishing a reference voltage (Nbias) on the line **309**. The reference voltage (Nbias) on the line **309**, as well as a supply voltage (Vdd) on a line **309'**, are provided to a current-scaling circuit **310**.

The supply voltage (Vdd) on the line **309'** is provided in any suitable manner, such as a multiple of a bandgap voltage (Vbg) generated in a conventional manner elsewhere on the chip, and its magnitude (e.g., 1.32 volts) should be independent of temperature, such as inherent to the silicon process which is employed in making the chip. The provision of such a stable (e.g., bandgap) voltage (e.g., Vbg) and the supply voltage (e.g., Vdd) derived therefrom is well within the purview of one having ordinary skill in the art to which the present invention most nearly pertains, and is described in greater detail hereinbelow with respect to FIG. 3B.

The current-scaling circuit **310** is constructed in the following exemplary manner. The sources of the transistors

P5 and P6 are connected to supply voltage Vdd. The gate of a transistor N6 receives the reference voltage (Nbias) on the line **309**. The transistor N6 is connected in a current-mirroring configuration with the transistor N5 (as well as with the aforementioned transistor N4) and will therefore mirror the flow of current I(T) through the transistors N4 and N5. Consequently, the flow of current through the diode-connected transistor P5 will mirror the flow of current through the transistors N4, N5 and N6.

The transistors P5 and P6 are connected in a current-mirroring configuration, but are fabricated (using conventional CMOS fabrication techniques) such that current flowing through the transistor P6 is scaled up or down by a ratio (N) of the physical area of the transistor P5 to the physical area of the transistor P6. For example, if the transistor P6 is smaller in size than the transistor P5 (i.e, the transistor P5 is "N" times larger in area than the transistor P6), then the current flowing through the transistor P6 will be commensurately (N times) smaller than the current flowing through the transistor PS. Thus, the "scaled" current flowing through the transistor P6, is labeled "I(T)/N" in the figure, and is provided on a line **311** to a relaxation oscillator circuit **312**. It is well known that the ratio of the currents between the transistors PS and P6 can readily be established by conventional circuit processing techniques, such as by simply making one of the transistors larger than the other, or by implementing a one of the two transistors as the aggregate of two or more same-size transistors so that their aggregate area is larger than the area of the other of the two transistors.

The relaxation oscillator circuit **312** is of fairly conventional design, and includes two pair of transistors at the "front end" of each of its two phase paths—a pair of complementary transistors P7 and N7 at the front end of a one phase path (ϕ1) **314***a*, and another pair of complementary transistors P8 and N8 at the front end of another phase path (ϕ2) **314***b*.

Connected as illustrated, for a given pair of transistors (e.g., P7 and N7), when with their common gate voltage is high (i.e., towards positive supply) their output will be grounded, and when their common gate voltage is low they will provide the current I(T)/N flowing on the line **311** to a respective one of the phase paths (e.g., **314***a*) of the relaxation oscillator **312**. As is known, in such an arrangement, when the common gate voltage of a one of the pairs of transistors (e.g., P7 and N7) is high, the common gate voltage of the other of the pairs of transistors (e.g., P8 and N8) will be low, and vice-versa. In this manner, each phase path **314***a* and **314***b* has a duty cycle (i.e., its "on" time), which may be the same as or may be different than the duty cycle of the other phase path **314***b* and **314***a*, respectively. Thus, each pair of transistors (e.g., P7 and N7) may be considered to be an "input switch" to its respective phase path (e.g., **314***a*).

Each phase path **314***a* and **314***b* of the relaxation oscillator **312** has a comparator **316***a* and **316***b*, respectively, at its input, and has a fixed-value capacitor C_{FX1} and C_{FX2}, respectively, connected between the negative (–) input of the comparators **316***a* and **316***b* and ground. The capacitors C_{FX1} and C_{FX2} have exemplary capacitance values of 2–5 pf (picofarads) and 2–5 pf, respectively, and are preferably implemented as "on-chip" devices, such as poly-to-poly capacitors exhibiting a low temperature coefficient (e.g., less than 20 ppm). The positive (+) inputs (terminals) of the comparators **316***a* and **316***b* are tied together and are set to a reference threshold voltage Vbg, such as 1.32 volts, which is independent of temperature.

A "NOR" logic gate **318***a* and **318***b* is connected at the output of each phase path **314***a* and **314***b*, respectively, and the two NOR gates **318***a* and **318***b* are cross-connected to form a latching circuit having an output on a line **319**. The cross-connected NOR gates **318***a* and **318***b* are thus capable of functioning as a flip flop, or an RS (re-set/set) latch.

When the common gate voltage of one of the input switches (e.g., P7 and N7) is high, the respective capacitor (e.g., C_{FX1}) for that phase path (e.g., **314***a*) is grounded (shorted out, caused to be devoid of charge). Conversely, when the common gate voltage of one of the input switches (e.g., P7 and N7) is high, the scaled current I(T)/N is applied to (allowed to flow into) the respective capacitor (e.g., C_{FX1}) for that phase path (e.g., **314***a*), and the capacitor and it begins to charge (acquire an increasing voltage across the capacitor). When the voltage across the capacitor reaches the comparator reference voltage (e.g., 1.32 volts) the output of the comparator goes low and changes the state of the output of the latch **318***a*/**318***b* on the line **319**. In this manner, the relaxation oscillator will oscillate at a frequency (Fosc) determined by the rise time of the capacitors C_{FX1} and C_{FX2} and, importantly, by the scaled current I(T)/N being supplied to the capacitors C_{FX1} and C_{Fx2}. With greater current I(T)/N being supplied, the voltages of the capacitors C_{FX1} and C_{FX2} will rise faster, crossing the threshold voltage faster, and causing the relaxation oscillator **312** to oscillate faster, thereby increasing the frequency of the signal Fosc on the line **319**. The signal Fosc on the line **319** is inverted by an inverter **320**, as shown, to provide a signal Fosc' on the line **321**.

As described in greater detail hereinbelow, the oscillator **312** is controlled to run in two mutually-exclusive modes, a temperature-sensing mode (between times t0 and t1) and a pressure-sensing mode (between times t1 and t2), as controlled by the timing generator/sequencer **226**. The frequency of the oscillator output signal Fosc (and of Fosc') will be different in each of these two modes.

Generating Temperature and Pressure Signals

In the exemplary context of the transponder **200** being associated with a pneumatic tire, it is principally desirable to determine the pressure within the pneumatic tire. For example, a typical passenger vehicle tire may be properly inflated at about 32 psi (about 221 kp).

It is, for example, estimated that an approximate 10% decrease in fuel consumption could be realized if the pneumatic tires on vehicles were operated at their specified pressure. Although vehicle fleet operators are typically sensitive to this issue, and check and adjust tire pressure frequently, the average operator of a passenger vehicle is often less inclined to keep an eye on their tire pressure until, for example, the tire is visibly flattened out. In such cases, an LCD (liquid crystal display) readout or the like on the dashboard of a car could provide dynamic tire inflation information to the operator of a vehicle, the pneumatic tires of which are equipped with a transponder such as the one described herein. Of no less significance is the emergence of "run-flat" tires being marketed by various tire manufacturers. The Goodyear EMT (extended mobility tire) series of tires is an example of a run-flat tire, an overall purpose of which is to allow a driver to travel up to 50 miles (~120 kilometers) on a deflated tire, at "reasonable" operating speeds (e.g., 60 miles Per hour, or 144 kilometers per hour), while maintaining normal control over the vehicle. Such run-flat tires are generally well known, and do not form a portion of the present invention, per se. When running flat on a run-flat tire, it is particularly important that the driver be alerted to the fact that he or she is operating the vehicle on

"borrowed time" as indicated, principally, by an indication, whether visual or audio (e.g., a beep) that the tire is indeed flat and needs to be repaired or replaced at his or her earliest convenience.

By allowing the relaxation oscillator **312** to run, the frequency of its output signal Fosc (and Fosc') will be a function of the absolute temperature of (sensed by) the transistor Q1. This is true in both the temperature-sensing mode and the pressure-sensing mode of operation.

In the temperature-sensing mode, and in the case that the capacitance values for C_{FX1} and C_{FX2} are equal, which is preferred, the relaxation oscillator **312** will have a symmetrical (balanced, 50%) duty cycle. In the pressure-sensing mode, the pressure-sensing capacitor (C_P) **218** is switched by a semiconductor switch **350** across C_{FX2}, which changes the duty cycle and output frequency Fosc (and Fosc') of the relaxation oscillator.

In the temperature-sensing mode, only the fixed capacitors C_{FX1} and C_{FX2} are being alternately charged (and discharged) resulting in a 50% duty cycle with a period proportional to ambient temperature. In the pressure-sensing mode, the pressure-sensing capacitor (C_P) **218** is switched into phase path **314***b* of the oscillator **312**. Thus, for a given temperature, for the first half of the oscillator period the phase path **314***a* behaves in the same manner as in the temperature-sensing mode, and for the second half of the oscillator period the phase path **314***b* behaves in a manner that is proportional to the capacitance value of the fixed capacitor C_{FX2} plus the capacitance value of the pressure-sensing capacitor (C_P) **218**. This, in effect, slows down the oscillator and changes its duty cycle. The change in the duty cycle is indicative of the ratio of C_P to C_{FX2}. Thus, from the ratio of the two periods (with and without C_P in the circuit, it is straightforward to calculate what the additional capacitance C_P is, hence the sensed pressure. As described in greater detail hereinbelow, the temperature-dependency of the oscillator output in the pressure-sensing mode can be completely eliminated, in a straightforward manner.

The "slowing down" of the oscillator when the pressure-sensing capacitor (C_P) **218** is switched into the oscillator circuit results, inevitably, in there being relatively fewer oscillator output pulses (reduced output frequency) to count during a given pressure-measurement window (e.g., W_P) than during a similar-duration temperature-measurement window (e.g., W_T). In other words, a "slowed-down" oscillator will reduce that rate at which counts indicative of the parameter measurement are collected. In order to increase the resolution (quantity) of the counts (N_P) generated during the pressure-measurement window (W_P), it is contemplated that the pressure-measurement window (W_P) can be increased in size (changed in duration) so as to allow for the capture of an appropriate number of pressure counts in the pressure register **234**. This can readily be accomplished simply by establishing a larger (than otherwise) value for the time t2 which establishes the end of the pressure-measurement window (W_P) in the pressure-sensing mode (between times t1 and t2), as controlled by the timing generator/sequencer **226**. For example, the temperature-measurement window W_T (between times to and t1) can be on the order of several ones (e.g., eight) of milliseconds, and the pressure-measurement window W_P can be on the order of tens or dozens (e.g., forty) of milliseconds. Alternatively, it is contemplated that the scaled current (I(T)/N) flowing out of the current-scaling circuit **310** to the relaxation oscillator **312** could be increased during the pressure-measurement window (W_P) to increase the fundamental frequency of the relaxation oscillator **312**, thereby increasing the overall resolution of the pressure count. This can readily be accomplished, for example in the case of **P6** being smaller in size (area) than the transistor **P5**, simply by switching in a transistor **P6'** (not shown) in lieu of the transistor **P6**, the transistor **P6'** having a larger area than the transistor **P6** so that the ratio of the areas of the transistors PS and **P6** is closer to unity (i.e., less scaled down) and the current to the relaxation oscillator **312**, hence its counting rate, is increased. Such switching in of another transistor **P6'** is readily effected with a switch (not shown) comparable to the aforementioned switch **350** which switches in the pressure-sensing capacitor (C_P) **218**. One having ordinary skill in the art to which the present invention most nearly pertains will readily understand how to offset the "slowing down" of the oscillator when the pressure-sensing capacitor (C_P) **218** is switched into the oscillator circuit, in light of the teachings presented herein.

Measuring Parameters

When the transponder is powered up, temperature and pressure are continuously measured, and these measurements are transmitted back to the external reader/interrogator **(106)** as data words in a data stream. For example, each of the temperature and pressure parameters can be transmitted back to the reader/interrogator **(106)** as 12-bit data words as selected (known) portions of a larger (e.g., 144-bit) data stream. One bit in the overall data stream may be dedicated to the state (e.g., "closed" or "open") of the MTMS switch **(220)**. A complete description of an exemplary data stream being transmitted by the transponder to the external reader/interrogator is set forth hereinbelow with reference to FIG. 3C.

Temperature is suitably measured by counting the number of cycles output from the oscillator **312** during a fixed time period (window of time from t0 to t1)) with a period T_W. For example, a down-counter (associated with the temperature register **(232)**) may be clocked by the oscillator, such that at the end of the window W_T, a temperature count N_T is generated. The relationship between N_T and temperature is linear.

Optimizing Pressure-Responsiveness

Obtaining (and displaying) an accurate pressure reading being of paramount importance when monitoring the pressure of a pneumatic tire, certain parameters of the transponder circuit may be established to maximize its pressure-responsiveness and therefore improve the accuracy of the pressure reading displayed by the external reader/interrogator **(106)**.

As described hereinabove, the transponder responds to the changing capacitance of the pressure sensor (C_P) **218** by changing the value of a binary 12-bit word that is transmitted to the external reader/interrogator **(106)**. This binary word is the count of an oscillator frequency during a timing window W_P (between t1 and t2) established by the timing generator/sequencer **226**. The pressure response can therefore be described as the change in counts per unit change in capacitance of the pressure-sensing capacitor (C_P) **218**.

Pressure-responsiveness of the transponder has been found to be dependent on a number of factors, each of which can be analyzed. For example, it has been determined that:

(a) increasing the scaled current I(T)/N to the oscillator **312** will proportionally increase the pressure counts N_P for a given value of the pressure-sensing capacitor (C_P) **218**; and

(b) decreasing the values for C_{FX1} and C_{FX2} will proportionally increase the pressure counts N_P for a given value of the pressure-sensing capacitor (C_P) **218**; and

(c) increasing the current I(T)/N to the oscillator will proportionally increase the pressure counts N_P (for a given value of C_P) at a greater rate than decreasing the values for C_{FX1} and C_{FX2}.

As a general proposition, increasing the pressure counts N_P is desirable. However, one having ordinary skill in the art to which the present invention most nearly pertains will readily appreciate that there is a practical upper limit to increasing the pressure counts at a frequency which may become unacceptably large for the capability of certain circuits of the IC chip.

Obtaining a Pressure Reading at the Reader/Interrogator

The fundamental frequency of the oscillator **312** is set by parameters in the IC chip (e.g., **204**) and, as described hereinabove, is temperature-dependent. Therefore, the pressure-response is a function (hybrid) of both temperature and pressure, and the relationship of N_P to C_P is nonlinear. Therefore, using a linear equation for calculating the pressure response would inevitably lead to significant errors over a range of pressures being measured. (For limited ranges of pressures being measured, for example over a 20 psi (138 kp) range of pressures, using a linear equation may, however, be acceptable.)

An important advantage of using the transponder circuitry described hereinabove is that the relationship between N_T/N_P to pressure sensor capacitance is linear, and requires no temperature compensation term in the equation (algorithm) used by the reader/interrogator (**106**) to calculate pressure, thereby greatly simplifying the design of the reader/interrogator. This beneficial "ratiometric" relationship is readily demonstrated by the following equations:

$$N_T = T_W * I(t)/(2 * Vbg * C_{FX}) \quad \text{(eqn. 1)}$$

$$N_P = T_W * I(t)/(Vbg * (2 * C_{FX} + C_P)) \quad \text{(eqn. 2)}$$

solving for N_T/N_P, the following is arrived at:

$$N_T/N_P = 1 + (C_P/2 * C_{FX}) \quad \text{(eqn. 3)}$$

It can thus be observed that the ratio N_T/N_P is only a function of C_P and C_{FX}, and no other variables. This means that N_T/N_P is only a function of pressure, and is insensitive to temperature or charging current variations.

FIG. 3A illustrates the components involved in the final step of capturing temperature and pressure measurements in the transponder. The signal Fosc' output by the relaxation oscillator **312** is provided to an input of each of two AND gates **360** and **362**. A signal ("Capture Temp") is provided by the timing generator/sequencer **226** to the other input of the AND gate **360** during the temperature-sensing window (W_T) so as to load the temperature register/counter **232** with the count (data) N_T indicative of measured temperature. Another data signal ("Capture Press") is provided by the timing generator/sequencer **226** to the other input of the AND gate **362** during the pressure-sensing window (W_T) so as to load the pressure register/counter **234** with the count (data) N_P indicative of measured pressure. These signals are then shifted out of the registers **232** and **234**, via the MUX **240**, to the modulation circuit **246** described hereinabove.

Generating Reliable Supply and Reference Voltages

As described hereinabove, the positive (+) inputs (terminals) of the comparators **316***a* and **316***b* are tied together and are set to a reference "bandgap" voltage Vbg, such as 1.32 volts, which is independent of temperature. As also mentioned hereinabove, the supply voltage (Vdd) on the line **309'** may be provided as a multiple of the reference bandgap voltage (Vbg) so as to be a stable operating voltage for the current steering circuit **310** and the relaxation oscillator **312**.

FIG. 3B illustrates a circuit **370** suitable for generating supply voltage Vdd. A temperature-independent calculable bandgap voltage Vbg is readily derived, based on the processing techniques employed in fabricating the IC chip, as being inherent to the selected process (e.g., CMOS). This bandgap voltage Vbg is provided to the "+" input of an operational amplifier **372**, connected as shown, in a feedback loop having gain, to provide supply voltage Vdd as an integral multiple of the bandgap voltage Vbg.

An Exemplary Data Stream

As mentioned hereinabove, information (data) from the transponder is transmitted to the external reader/interrogator in the form of a data stream, a portion of which is the temperature count N_T, another portion of which is the pressure count N_P, and another portion of which represents the state (e.g., "closed" or "open") of the MTMS switch (**220**). Remaining portions of the data stream may contain information which is personalized to a given transponder unit such as its ID information (e.g., serial number), calibration constants, and the like.

FIG. 3C illustrates an exemplary architecture for information which is stored (in memory) within the transponder, as well as a data stream which is transmitted by the transponder to the external reader/interrogator. The memory of the transponder core **204** has, for example, a 144-bit address space which includes 119 (one hundred nineteen) bits of programmable memory and one address location dedicated to the state of the MTMS switch **220**, these 120 (one hundred twenty) bits of programmable memory constituting the EEPROM (**136**), plus the two 12-bit registers **232** and **234**.

Each of the 119 programmable memory bits can separately be written to with any combination of data, including synchronization (sync) pattern information, general data, error checking codes, and temperature and pressure calibration data. The EEPROM is 'block writeable', meaning that in the 'write' mode, the entire 120 bits of EEPROM are programmed to a logical (binary) value of "1". Individual bits can be 'erased', or set to a logical value of "0" simply by clocking the chip to its physical address and placing the chip into the 'erase' mode. The address location is preserved.

In this example, the first twelve data locations (000 . . . 011) in ROW **1** are reserved for sync. The next seventy one data locations (012 . . . 082) in ROWs **2** through **7** are for general information and a value for a data validation algorithm such as CRC (Cyclic Redundancy Check). The next data location (**083**) contains the logic level (state) of the MTMS switch **220**. A logical value of "1" indicates that the MTMS switch is open and a logical value of "0" indicates that the MTMS switch is closed.

The transponder unit is suitably calibrated prior to its installation in a tire. This basically involves determining slope and intercepts for temperature and pressure values generated by the transponder at various temperatures and pressures in a test chamber, and programming these characteristic calibration values associated with the transponder into the memory space. The next twelve data locations (084 . . . 095) in ROW **8** hold temperature calibration (e.g., intercept) data ("TEMP COMP"). The next twelve data locations (096 . . . 107) in ROW **9** hold pressure calibration (e.g., intercept) data ("PRESS COMP"). The next twelve data locations (108 . . . 113 and 114 . . . 119) in ROW **10** hold calibration slope information for temperature and pressure, respectively.

According to an aspect of the invention, it has been determined that characteristic values for the slope of the

N_T/N_P, or "ratioed" response of temperature count divided by pressure count, is linear with respect to the value of the pressure-sensing capacitor C_P, and using this ratioed value of N_T/N_P requires no temperature compensation term in an equation used to calculate pressure. Additionally, it has been determined that the ratioed value of N_T/N_P is less sensitive to variations in coupling between the reader/interrogator and the transponder than either of these measurements taken alone. Thus, by determining (during calibration) and storing calibration data for the ratioed value of N_T/N_P in the transponder, the ability to determine a true pressure reading which is relatively insensitive to coupling variations between the reader/interrogator and the transponder is both simplified and made more reliable. This ratioed calibration value for N_T/N_P is stored in the transponder memory and included in the data stream transmitted to the external reader/interrogator.

As counts N_T and N_P for temperature and pressure are generated, as described hereinabove, they are stored in ROWs 11 and 12 of the overall memory space, which correspond to the temperature and pressure registers 312 and 314, respectively. Various predetermined values can be stored to indicate overflow and short-circuit conditions.

Operating Frequencies and Modulation

The transponder of the present invention is not limited to any particular operating frequency. The choice of operating frequency will depend largely upon factors such as where the transponder is mounted, in relationship to the object it is monitoring, the location of the reader antenna (108), and relevant government regulations permitting (conversely, restricting) data transmissions of the type set forth herein in selected portions of the overall RF frequency spectrum.

An example of suitable operating frequencies for operating the transponder in the United States is 60 KHz to 490 KHz.

The transponder can be polled (and powered) by the reader/interrogator at an first "interrogation" frequency (Fi), and the data stream can be transmitted back to the reader/interrogator at a second "data carrier" frequency (Fc) which is, conveniently, a whole number multiple or fraction of the interrogating frequency. For example, Fc=Fi/2. Or, Fc=Fi/4. The frequency (Fc) at which the data stream is transmitted back to the reader/interrogator is independent of the data rate, which is established by the clock generator 224 and the baud rate generator 248. However, one having ordinary skill in the art to which the present invention most nearly pertains will recognize that the range of available baud rates will typically be significantly less than the interrogation frequency (Fi). The baud rate is preferably derived from the interrogation frequency (Fi) of the reader/interrogator, such as a whole number fraction thereof. For example, the baud rate may be set at Fi/32 (or, in the case of Fc=Fi/2, the baud rate can be set to Fc/16).

For example, the interrogation frequency (Fi) may be 125 KHz, and the data carrier (Fc) may be set to 62.5 KHz, or half of the interrogation frequency.

In another example, an interrogation frequency (Fi) of 13.56 MHz has been found to be suitable.

The data stream, such as the exemplary data stream described with respect to FIG. 3C is impressed by the modulator circuit 246 onto the antenna 212, and transmitted to the reader/interrogator. It is within the scope of this invention that any suitable modulation scheme be employed, including amplitude modulation (AM), frequency modulation (FM), frequency shift keying (FSK), and phase shift keying (PSK). However, phase shift keyed (PSK) is preferred. AM modulation is not particularly well-suited to digital transmission. Frequency modulation schemes such as FM or FSK may be somewhat problematic with regard to propagating the data-modulated transponder output signal through the medium of a pneumatic tire.

Obtaining a Temperature-Compensated Pressure Reading

FIG. 4 illustrates a relevant portion of a reader portion of a reader/interrogator 400. It should clearly be understood that the transponder of the present invention is suitable for use with virtually any suitably configured reader interrogator. The description that follows is limited to broad architectural functions that would be performed in the reader/interrogator. One having ordinary skill in the art to which the present invention most nearly pertains would be able, from the description set forth herein, to implement these functions in an otherwise "generic" reader/interrogator.

The data-modulated transponder output signal is received by the antenna 410 (compare 210) of the reader/interrogator 400 (compare 200). The received signal is de-modulated and de-coded in a de-modulator/decoder circuit 420 (DE-MOD/DECODE) so that the different portions of the data stream can be properly segregated from one another. The data relating to temperature and pressure calibration (TEMP COMP, PRESS COMP, TEMP/PRESS SLOPES), the temperature count (NT) and the pressure count (N_P) are provided to an arithmetic logic unit 422 capable of generating a true, temperature-compensated pressure signal ("PRESSURE") on a line 423 to the display 412 (compare 112) as well as a calibrated temperature signal ("TEMPERATURE") on the line 423. This information can be displayed to the user either selectively or simultaneously with other relevant information such as the state of the MTMS switch 220, as well as data (DATA) relating to tire identification and the like.

While the invention has been described in combination with embodiments thereof, it is evident that many alternatives, modifications, and variations will be apparent to those skilled in the art in light of the foregoing description. Accordingly, the invention is intended to embrace all such alternatives, modifications and variations as fall within the spirit and broad scope of the appended claims.

What is claimed is:

1. A method of measuring temperature utilizing an integrated circuit (IC) chip, the method comprising:

flowing a current through a resistor (Rext), the resistance value of which is substantially independent of temperature, said current being a function of an absolute temperature of a transistor (Q1) resident on the IC chip, said transistor being of a type which exhibits a predictable change in its base-emitter voltage over a temperature range;

mirroring the current flowing through the resistor to a circuit on the IC chip, said circuit providing an output signal which is proportional to the current flowing through the resistor, thereby making the output signal temperature-dependent as a function of the absolute temperature of the transistor;

including at least one internal capacitor in the circuit and an external capacitor outside the circuit; and

selectively switching the external capacitor across the at least one internal capacitor to alter a characteristic of the output signal.

2. The method of claim 1, wherein:

the circuit is a relaxation oscillator, and the output of the circuit is a temperature-dependent frequency.

* * * * *

APPENDIX F

***Hodemaekers* Reference**

U.S. Patent No. 4,298,866

United States Patent [19]

Hodemaekers

[11] **4,298,866**

[45] **Nov. 3, 1981**

[54] **LIQUID CRYSTAL DISPLAY DEVICE HAVING CAPACITANCE COMPENSATION**

[75] Inventor: **Andreas M. L. Hodemaekers**, Eindhoven, Netherlands

[73] Assignee: **U.S. Philips Corporation**, New York, N.Y.

[21] Appl. No.: **91,429**

[22] Filed: **Nov. 5, 1979**

[30] **Foreign Application Priority Data**

Dec. 15, 1978 [NL] Netherlands 7812214

[51] **Int. Cl.**[3] **G06F 3/14**

[52] **U.S. Cl.** ..... **340/713**; 340/784; 350/331 T

[58] **Field of Search** ..... 340/713, 784; 350/331 R, 331 T, 332, 336

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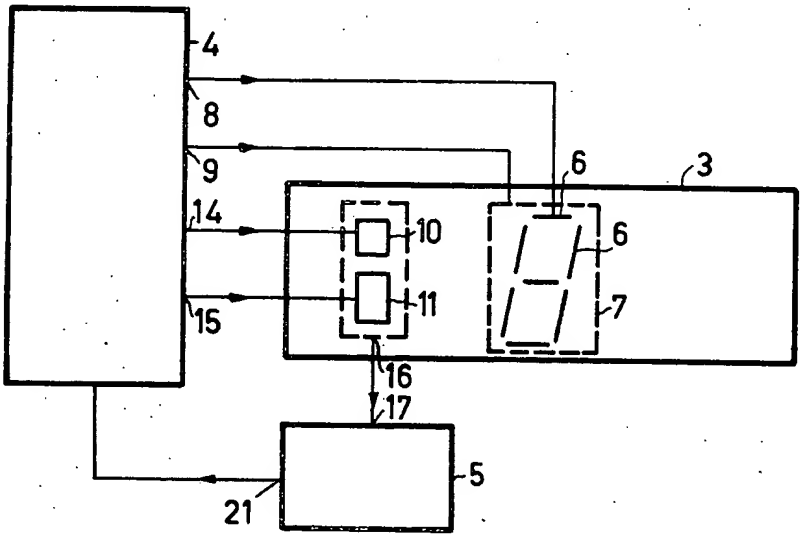
Primary Examiner—Marshall M. Curtis
Attorney, Agent, or Firm—Thomas A. Briody; Robert T. Mayer; Paul R. Miller

[57] **ABSTRACT**

A display apparatus having a liquid crystal display is provided with a measuring element for controlling the drive voltages depending on the temperature of the liquid crystal. The effect of manufacturing tolerances and ageing phenomena are compensated for by means of an auxiliary measuring element. The electric voltages across the measuring element and the auxiliary measuring element differ from one another, for the adjustment of mutually different operating points on the capacitance-voltage curve.

7 Claims, 5 Drawing Figures



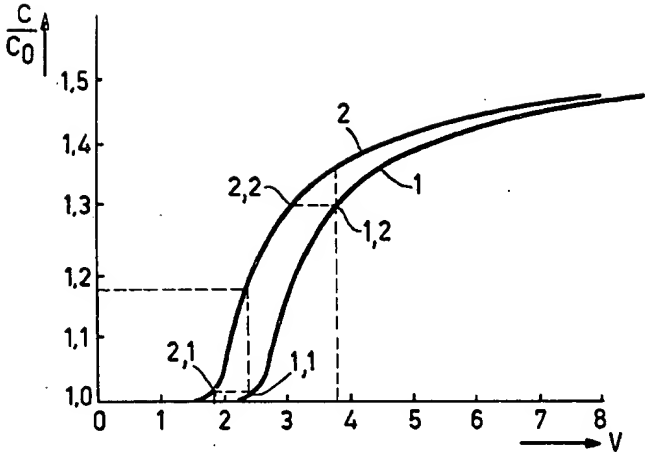


FIG.1

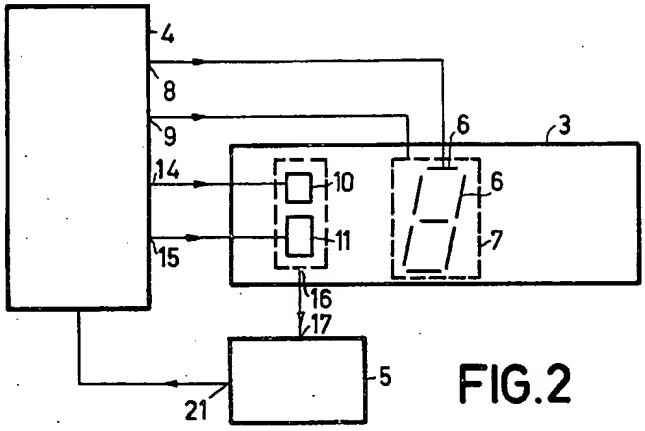


FIG.2

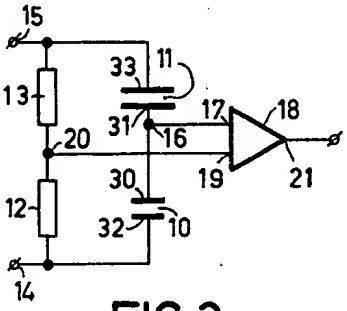


FIG.3

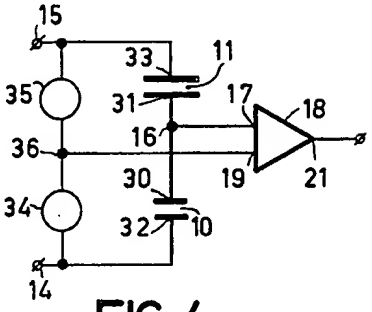


FIG.4

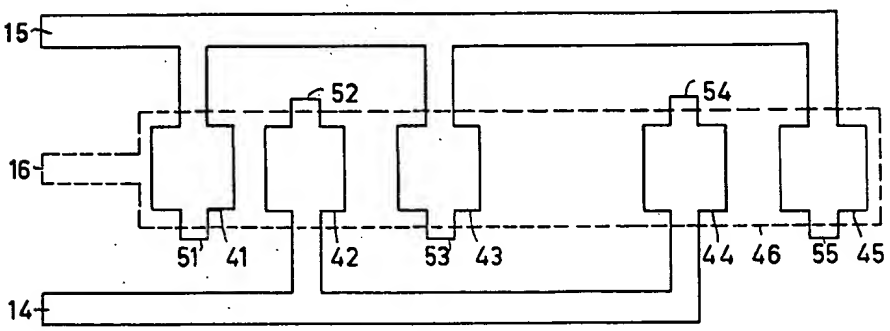


FIG.5

LIQUID CRYSTAL DISPLAY DEVICE HAVING CAPACITANCE COMPENSATION

The invention relates to a display device comprising a display screen having a plurality of display elements and a measuring element, the display screen comprising a liquid crystal enclosed between a first and a second cover plate each having a plurality of excitation electrodes for feeding electric display drive voltages to the display elements and an electric measuring drive voltage to the measuring element;

an excitation circuit for generating the display drive voltages and the measuring drive voltage; and

a control circuit having at least a measuring input for an electric measuring signal, this measuring input being coupled to one of the excitation electrodes of the measuring element, and having at least a control output for an electric control signal;

which control circuit adjusts the amplitude of the display drive voltages and of the measuring drive voltage to the values corresponding to the threshold voltage of the liquid crystal in response to impedance variations of the measuring element resulting from the temperature and voltage dependence of the liquid crystal.

Such display devices are frequently used for displaying alpha-numerical information in data processing systems, measuring instruments etc. The symbols to be displayed can be displayed either in the form of a dot matrix or, alternatively, by means of a 7-segment pattern. In both cases excitation will usually be effected by means of a matrix control circuit, the individual display elements being operated in time-division multiplex.

With such a control the so-called multiplex factor will remain very low, usually limited to 2 or 3, if no special measures are taken, as the attainable multiplex factor depends on the difference between the voltages V_{ON} and V_{OFF} which are required, as apparent from the contrast-voltage curve, to achieve a sufficiently high contrast.

A high multiplex factor would be attainable with a sufficiently steep contrast-voltage curve but for the fact that the threshold voltage is always highly temperature-dependent. In the required temperature range the difference between the highest V_{ON} occurring in this temperature range and the lowest V_{OFF} are decisive for the attainable multiplex factor. In a display device of the type defined above this drawback is obviated to a considerable extent by adapting the amplitude of the excitation signals to the instantaneous values of V_{ON} and V_{OFF}.

Also when the display device is not operated in time-division multiplex, temperature variations can be very disturbing if, for example, only very low supply voltages are available, as is inter alia the case for wrist watches, or if a very wide temperature range is required, as is inter alia the case for display devices in motor cars. A display device of the type defined in the preamble is known from "A novel method of temperature compensation for multiplexed liquid crystal displays", Electronic Letters, July 6, 1978, volume 14, No. 14, pages 430 and 431, FIG. 3 in particular.

This publication describes a display device in which a measuring element G_{LC} is included in the display screen, the measuring element being arranged in series with an impedance Z in the control circuit. The a.c. voltage across the measuring element is used as the control voltage for adapting the amplitude of the excitation signals. This is possible because the capacitance-voltage curve of an element of the liquid crystal varies analogously with the contrast-voltage curve and shifts in the same manner along the direction of the voltage axis in response to temperature variations.

Although a proper temperature compensation can be achieved initially, it appears that in this system each display screen requires an individual adjustment. The capacitance of the measuring element C_{LC} depends inter alia on manufacturing tolerances in the specifications of the liquid crystal and in the mechanical implementation of the display screen, particularly the average distance between the first and the second cover plate playing an important role.

In addition it appeared that the capacitance value at a certain temperature and voltage also varies due to ageing, so that the adjustment during the life of the display apparatus must be frequently corrected.

It is an object of the invention to provide a display apparatus wherein no adjustment is required to compensate for any differences between devices of one and the same type or variations in time.

According to the invention a display device of the type mentioned in the preamble is therefore characterized in that the display screen also comprises an auxiliary measuring element, the size of which differs from that of the measuring element, the auxiliary measuring element being arranged in series with the measuring element, with ends of this series arrangement being coupled to the excitation circuit for supplying the measuring drive voltage, and the junction of the measuring element and the auxiliary measuring element being coupled to the measuring input of the control circuit.

In a display device in accordance with the invention the ratio of the capacitances of measuring element and auxiliary measuring element are therefore not affected in the first order by tolerances in the properties of the liquid crystal or in the mechanical implementation of the display screen, as the percentages of the influences thereof are the same for both capacitors so that these tolerances do not affect the ratio of the electric voltage at the junction of the measuring element and the auxiliary measuring element and the measuring drive voltage. This also holds for deviations which may be caused by ageing of the display screen, for example, because the distance between the first and the second cover plate changes gradually.

As the measuring element and the auxiliary measuring element differ in size the electric voltages across these elements become unequal in the series arrangement. They are both capacitors having a portion of the liquid crystal as the dielectric, so that the capacitance as well as the parallel resistance of these capacitors are highly temperature-dependent, the predominant part being played by the capacitance, also because excitation is preferably effected by means of a.c. voltages in view of the required life time of the liquid crystal.

The relevant temperatures being the same, the measuring element and auxiliary measuring element are adjusted to different operating points of the capacitance-voltage curve owing to the mutually different voltages across the elements. The result thereof is that at a constant measuring drive voltage the capacitance values will change to a different extent in response to a change in the temperature, so that the ratio between the voltage at the junction and the measuring drive voltage changes.

By varying the measuring drive voltage the original ratio can thereafter be obtained again. This control is effected by using the voltage at the junction for a negative feedback control system in a manner which is known per se.

In this manner, with a sufficiently high loop gain in the control circuit, the influence of temperature variations on the setting of the liquid crystal can be made negligibly small over a wide temperature range.

An advantageous display device in accordance with the invention is furthermore characterized in that the control circuit comprises

a differential amplifier, a first and a second signal input which constitute a first and a second measuring input of the control circuit; and

a further series arrangement of a first and a second bridge impedance, ends of this further series arrangement being connected to the ends of the series arrangement of the measuring element and the auxiliary measuring element for forming a bridge circuit,

wherein the junction of the measuring element and the auxiliary measuring element is coupled to the first measuring input and the junction of the first and the second bridge impedance is coupled to the second measuring input.

This control amplifier now compares the voltage at the junction of the measuring element and the auxiliary measuring element with the voltage at the junction of the two bridge impedances. So this latter voltage functions as the reference voltage. The ratio of this reference voltage to the measuring drive voltage can be chosen equal, using impedances of a sufficient precision for all devices of a production series, due to the fact that manufacturing tolerances cannot play an important role in the ratio of the capacitance values of the measuring element and the auxiliary measuring element.

Resistors can be used for the impedances, alternatively, for example, in the form of a fixed-tap resistor, co-integrated in an integrated circuit.

A further advantageous display device in accordance with the invention is characterized in that

the control circuit comprises a differential amplifier, a first and a second signal input which constitute a first and a second measuring input of the control circuit; and

the excitation circuit comprises a series arrangement of a first and a second electric voltage source for producing the measuring drive voltage;

wherein the junction of the measuring element and the auxiliary measuring element is coupled to the first measuring input and the junction of the first and the second voltage source is coupled to the second measuring input.

Herein the junction of the two voltage sources serve as the reference point for the control circuit. In all other respects the operation of this device is equivalent to the operation of the display device previously described.

Generally, the electrodes of the measuring element and the auxiliary measuring element together with the required electric connections as well as the electrodes of the display elements will be provided in the form of printed circuits onto the first and the second cover plates. It is then possible that, owing to tolerance errors in the preparation of drawings, photographs, printing masks etc. for production processes the ratio of the capacitance values does not fully correspond to the ratio of the two fixed reference elements, which last ratio can be known very accurately when precision components are used. To render the influence of this further tolerance problem negligibly small a further advantageous display device in accordance with the invention is characterized in that the measuring element and the auxiliary measuring element are formed from a number of equal and identical basic elements.

Only one of the basic elements need be drawn in the preparation stage whereas the other elements can be obtained by means of a repeating mechanism which is known per se. Should any drawing tolerances occur, they will now be exactly the same for all basic elements and therefore do not play any part in the adjustment of the bridge circuit.

In this last-mentioned case the two capacitance values will always be related as single integral numbers. This is no essential restriction as the ratio can be freely chosen between wide limits. If, for example, a ratio 1,5 is chosen, the smallest of the two measuring elements may, for example, consist of a parallel arrangement of 4 basic elements and the largest element of a parallel arrangement of 6 basic elements.

For large display screens, such as inter alia elongate display screens for measuring instruments, the thickness of the liquid crystal layer may vary somewhat owing to assembly tolerances, which might again affect the capacitance ratio. To obviate this, a further display device in accordance with the invention is characterized in that the basic elements are distributed evenly over the display screen.

Generally, the required excitation signals, the measuring excitation signal included, will be generated by means of electric circuits which are fed by one common supply unit. A very simple control feature is obtained when the excitation circuit is of a type wherein the amplitudes of the drive voltages, generated by the excitation circuit are predominantly proportional to a supply voltage applied to the excitation circuit, a supply input of the excitation circuit being connected to a supply output of a controllable supply unit having a control input for an electric control signal, this control input being coupled to the control output of the control circuit.

Adjusting the output voltage of the supply unit by means of an external control signal is done in a manner which is known per se, wherein, for example, the output signal of the differential amplifier is applied to the supply unit after having been rectified.

Embodiments of the invention will now be described by way of example, with reference to the drawings.

In the drawings:

FIG. 1 shows two capacitance-voltage curves of a liquid crystal element with temperature of the liquid crystal being used as a parameter;

FIG. 2 shows a simplified block diagram of a display device in accordance with the invention;

FIG. 3 shows a simplified circuit diagram of a bridge circuit having a first and a second bridge impedance.

FIG. 4 shows a simplified circuit diagram of a bridge circuit having a first and a second voltage source, arranged in series therewith, for supplying the measuring drive voltage; and

FIG. 5 is an example of an advantageous electrode configuration for the measuring element and the auxiliary measuring element.

FIG. 1 shows two capacitance-voltage curves 1 and 2 for a twisted nematic liquid crystal for two different temperatures T_1 and T_2, respectively, of the liquid crystal, in an adapted shape taken from Meyerhofer, Mol. Cryst. Liq. Cryst, 1976, volume 34 (Letters), pages

13-17. However, the invention is in no way limited to liquid crystals of this type as it also holds for other types that a change in the molecule orientation in response to the application of a sufficiently strong electric field produces a change in the dielectric constant of the liquid crystal and therefore, simultaneously therewith, a change in the capacitance values of the measuring elements as well as of the display elements. This also holds for liquid crystals which are not of the so-called "root-mean-square" type, for which the amplitude of the drive voltage must be taken for the voltage along the X-axis of the Figure instead of the r.m.s. value across the element.

The relative capacitance value C of an element with respect to the initial value C_O occurring at very low voltages is plotted on the vertical axis.

This relative capacitance value does not change considerably until it has reached a threshold voltage V_{th}, that is to say at the same V_{th} which indicates the instant in the contrast-voltage curve at which the change in the molecule orientation begins. The curve **1** shows the curve for a temperature T_1, the curve **2** the curve for a higher temperature T_2 having threshold values V_{th1} and V_{th2}, respectively, of approximately 2.3 and 1.8 V, respectively, in this example. An element of the liquid crystal is driven for display purposes by a (rms) a.c. voltage V, whose value varies between a voltage V_{OFF} and a voltage V_{ON}. Generally, a value approximately equal to or lower than V_{th} is chosen for the voltage V_{OFF}, it being possible to use a value somewhat higher than V_{th} without the occurrence of an annoying reduction in contrast. Hereinafter it is assumed, for simplicity, that $V_{OFF}=V_{th}$. The value $V_{ON}>V_{OFF}$ is determined by the desired attainable contrast. In FIG. **1** the point **1,1** indicates V_{OFF} and **1,2** indicates V_{ON}. Generally, it is sufficient to choose the value for V_{ON} in this manner for one distinct temperature T_i and to assume furthermore that $V_{ON}=aV_{th}$ wherein the constant a corresponds to:

$$a = \frac{V_{ON,i}}{V_{th,i}}$$

If a voltage V_{OFF} or lower is applied to the element, the molecules will be in the rest condition; however, depending on the optical auxiliary means of observation, such as crossed polarizers or non-crossed polarizers, illumination by means of transmitted or incident light and on the chosen type of liquid crystal this may mean that the relevant element display itself to the viewer, as a light segment or display dot against a dark background and may, consequently, visually give the impression of being in the "ON"-state. So the designations V_{OFF} and V_{ON} are coupled to the rest condition and the "operating" condition, respectively, of the molecules and need therefor not correspond to visual "OFF" and "ON", respectively, of a display element.

If the voltages across the two elements are in the ratio of, for example, 1:1.5 it can be seen from the graph that the capacitance of the measuring element will increase at the higher temperature at otherwise unchanged voltages from 1.02 $C_{M,O}$ to approximately 1.18 $C_{M,O}$, whereas the capacitance of the auxiliary element does not yet increase. $NC_{M,O}$ is the capacitance of the measuring element at very low voltages.

In reality however the voltage distribution across the two elements will change. The changed voltage distribution allows the voltage V_m over the measuring element to be reduced to such an extent that the operating point of the measuring element with a capacitance C_M becomes located at the point **2,1** of curve **2**, that is to say at a voltage across the element of approximately 1.8 V instead of 2.3 V. The voltage across the auxiliary element is 1.5 times lower and consequently decreases from approximately 1.53 V to approximately 1.2 V, and the measuring drive voltage must therefore be reduced from $2.3+1.53=3.82$ V to $1.8+1.2=3.0$ V to reach this state.

FIG. **2** is a simplified block diagram of a display apparatus according to the invention having a display screen **3**, an excitation circuit **4** and a control circuit **5**. A portion of a number of display elements **6** of the display screen is shown in the form of electrodes, shown by means of a solid line, on the first cover plate and a common counter electrode **7**, shown by means of a dotted line, on the second cover plate. Shown are the connections for the top element **6** to the excitation circuit **4**, the first electrode of this display element being connected to an output **8** of the excitation circuit **4**. The second electrode or counter electrode **7** being connected to an output **9**.

In a manner, which is known per se a drive voltage V_{OFF} or V_{ON} is generated between the outputs **8** and **9**, depending on the information to be displayed.

In addition the display screen **3** comprises a measuring element **10** and an auxiliary measuring element **11** having a common counter electrode **16** which also constitutes the junction of measuring element **10** and auxiliary measuring element **11b**

The first electrodes of these two elements are connected to outputs **14** and **15**, respectively, of the excitation circuit **4**, it being possible to generate a measuring drive voltage V_m between these outputs.

The junction **16** is coupled to a measuring input **17** of the control circuit, which generates a control voltage at a control output **21** for the simultaneous control of the output voltages V_m, V_{OFF} and/or V_{ON} of the excitation circuit **4**.

Two embodiments of the coupling of measuring element **10** and auxiliary measuring element **11** to the input section of the control circuit **5** are discussed with reference to the FIGS. **3** and **4**. Corresponding components in the Figures have been given the same reference numerals.

FIG. **3** shows an example of a measuring element **10** having an initial capacitance value $C_{M,O}$, arranged in series with an auxiliary measuring element **11** having an initial capacitance value $C_{H,O}$ and included in a bridge circuit which further comprises two fixed impedances **12** and **13**, for example resistors having resistance values R_1 and R_2, respectively. A measuring drive a.c. voltage V_m is applied to the bridge circuit via the terminals **14** and **15**.

The tap **16** of the series arrangement of measuring element **10** and auxiliary measuring element **11** is coupled to a first input **17** of a differential amplifier **18**, which has a second input **19** coupled to a tap **20** of the series arrangement of the impedances **12**, **13** and an output **21** which constitutes the output for a control voltage.

$$V_R = k(V_{20} - V_{off})$$

where k is a constant and V_{20} the voltage across the impedance 12 and V the voltage across the auxiliary element 10.

The bridge circuit is in balance when

$$C_M/C_H=R_2/R_1$$

A simple system is obtained when R_1 and R_2 are chosen so that

$$R_2/R_1=C_{M,O}/C_{H,O}$$

in the example shown in the drawing $C_{H,O}>C_{M,O}$ but this is not essential. When $C_{H,O}<C_{M,O}$ the circuit operates in a similar manner, the difference being that the bridge output a.c. voltage will have the opposite polarity when the bridge balance is disturbed in response to a capacitance change.

It is clear that

$$V_{off}=\frac{C_H}{C_M+C_H}\cdot V_m$$

As long as $V_{off}<V_{th}$ the capacitors have a capacitance $C_{M,O}$ and $C_{H,O}$, respectively, so that the bridge circuit is in balance and $V_R=0$.

When V_m increases to such a value that V_{off} just exceeds V_{th} then the capacitance of the measuring element 10 will increase in accordance with FIG. 1 so that $C_M>C_{M,O}$. The voltage across the auxiliary measuring element 11 is equal to

$$V_H=\frac{C_M}{C_M+C_H}V_M=\frac{C_M}{C_H}V_{OFF}$$

and, consequently, V_H is still lower than V_{th}, so that $C_H=C_{H,O}$. The bridge is now out of balance and produces, after amplification, a control voltage $V_R\neq O$, which vigorously opposes in known manner a further increase of V_m in a negative feedback control system. This stabilizes the voltage V_{off} at a value which is always approximately equal to V_{th} and consequently generally also approximately equal or equal to V_{OFF}. At a temperature T_1 this results in a setting at which the operating point of the measuring element corresponds to the point 1,1 of curve 1 in FIG. 1.

Should the temperature increase to a value T_2 the bridge circuit becomes again unbalanced. The increase of the bridge output a.c. voltage now causes the excessive value of V_m to decrease until the setting of the measuring element substantially corresponds to the point 2,1 of the curve 2 in FIG. 1, the ratio of the capacitance values being equal to that set at the temperature T_1. Now the voltage across the measuring element is substantially equal to the new threshold voltage V_{th} which is associated with the curve 2.

By controlling the drive voltages V_{ON} and V_{OFF} in a similar manner as V_m, V_{OFF} will also substantially correspond at this new temperature to the point 2,1 of curve 2, whereas V_{ON} approximately corresponds to the point 2,2 of this curve.

Consequently the contrast occurring at the display elements is in a first approximation independent of the temperature.

So in this example the setting of V_m must satisfy

$$V_m=\frac{C_M+C_H}{C_H}V_{off}\frac{C_M+C_H}{C_H}V_{th},$$

whereas $V_{ON}=a\,V_{th}$.

If V_{ON}, V_{OFF} and V_m are all generated by means of the same controlled system, they are, for example, all in a fixed ratio to the supply voltage of a controlled power supply, one control voltage for all drive voltages will be sufficient. Generally, this is, for example, the case when the signals are generated by means of digital circuits.

When C_M and C_H are suitably chosen it is possible to achieve an adjusted value V_m that is also suitable for an other drive voltage in the display device. Even when the elements 10 and 11 are implemented from a plurality of parallel-arranged basic elements it is always possible to obtain a sufficiently proper approximation.

The invention idea does not require the bridge to be in balance at a voltage $V_{OFF}=V_{th}$.

Alternatively, $C_{H,O}$, $C_{M,O}$, R_1 and R_2 can be chosen so that the bridge is in balance for $V_{OFF}=V_A$, where, for example, $V_H>V^{th}$.

The bridge circuit will now be out of balance for all values of V_m, so that $V_{OFF}<V_A$, but the polarity of the bridge output voltage will be the opposite of voltages for which $V_{OFF}>V_A$. If, for example, V_R is rectified in a phase-dependent manner which is known per se, for example by means of a synchronous detection relative to V_m, then the rectified control voltage will, for example, pass from a negative value through zero to a positive value at an increasing V_m, as soon as V_{OFF} exceeds V_A.

It is alternatively possible to choose the bridge circuit so that it is in balance at a much higher V_m, for example thus that V_{OFF} stabilizes at a value approximately equal to V_{ON}, it only being a condition that the operating point of the control circuit is chosen to be in a position where the capacitance-voltage curve has a sufficiently pronounced curve, so not at or near the point of inflection of the curve.

An operating point at an area of the curve which is curved to a lesser extent than the area at and around V_{th} indeed requires a higher gain of the differential amplifier 18 and the terminals 17 and 19 of the amplifier 18 must possibly be interchanged or the polarity of the synchronous detection must, for example, be reversed for curves for which the second derivative gets the other sign.

The actual performance of such variations in the embodiment of a display device in accordance with the invention are fully within the capability of those skilled in the art.

It will be clear that neither the measuring element nor the auxiliary measuring element can serve as a display element which, depending on the information applied to the excitation circuit, must sometimes be visually ON, sometimes visually OFF. Depending on the chosen embodiment they are both either visually ON for the time the display device is in the switched-ON stage, or they are both constantly visually OFF.

In the first case the elements can be visually covered, for example by means of a frame around the display screen, or either one of the two elements or both can be used for the display of a figure which must be visually constantly ON, for example a frame or "box", a type indication or the emblem of a firm.

The second case does not require special measures. Particularly for large display screens it is then advantageous that the measuring element and auxiliary measuring element can be included in any arbitrary location between the picture display elements.

Generally it will be efficient to provide the interconnected electrodes **30, 31** on one and the same cover plate and the electrodes **32, 33** of the auxiliary elements on the other cover plate. However, this is not a requirement.

FIG. **4** shows an embodiment wherein the measuring drive signal V_m is produced by a series arrangement of two voltage sources **34** and **35**. When the ratios of the voltages V_1 and V_2 of these voltage sources are equal to the ratios of the impedances R_1 and R_2, respectively, of FIG. **3**, the voltage at the junction **36** of the two voltage sources will be the same as that at the junction **16** of FIG. **2**. In all other respects the circuit shown in FIG. **4** operates in the same manner as that shown in FIG. **3**.

The bridge circuit will be in balance when, for example:

$$R_2/R_1 = C_M/C_H$$

For a predetermined chosen setting then

$$C_M = a\, C_{M,O}$$

and

$$C_h = b\, C_{H,O}$$

If the setting has been chosen as shown in FIG. **1** then it follows, for example, that

a = 1.02

b = 1.00

So, generally

$$\frac{R_2}{R_1} = K\frac{C_{M,O}}{C_{H,O}}$$

for a chosen constant K = a/b.

As mentioned above the ratio of $C_{M,O}$ and $C_{H,O}$ are only determined by the ratios of the surface areas of measuring element **10** and auxiliary measuring element **11** and independent of manufacturing tolerances and ageing of the display scree. Once these surface areas have been drawn with a sufficient accuracy in the preproduction stage the ratios of R_2 and R_1 are therefore known, so that fixed resistors, generally having fixed impedances, are sufficient. It is then not necessary, to adjust each produced item individually nor to repeatedly adjust in the case of ageing.

The ratio $C_{M,O}/C_{H,O}$ can be chosen freely within wide limits. In the given example it is clear that the voltage across C_h is little important, as long as this voltage is sufficiently low with respect to V_{th}.

It will therefore always be possible to choose the surface areas of the measuring element so that the mutual ratio consists of single integral numbers. In that case the measuring elements can be formed by means of mutually equal basic elements having a surface area e.

When choosing the ratio to be 2, then one element can be formed by one basic element and the other one by means of two parallel-arranged basic elements, but, alternatively also by, for example, two parallel-arranged and four parallel-arranged basic elements, respectively.

A factor of 1.5, as mentioned above by way of example results in

$$\frac{C_{M,O}}{C_{H,O}} = \frac{2e}{3e} \text{ or } \frac{4e}{6e} \text{ etc.}$$

This now offers the possibility of eliminating a drawing tolerance in the pre-production stage as well. As the cover plates are implemented as printed circuits, a non-recurrent drawing of a basic element and its reproduction by means of a repetition device which is known per se, which is much more accurate than a renewed drawing by a draughtsman, will be sufficient.

FIG. **5** shows a configuration of five basic elements, arranged in parallel in groups of two and three basic elements, respectively, the basic elements **41, 43** and **45** having been arranged in parallel at one side by means of the conductor **15**, and the basic elements **42, 44** by means of the conductor **14**. A common counter electrode on the other cover plate is shown in outline by means of the dotted line **46** and is connected to the conductor **16**. So, as in FIG. **2**, the additional auxiliary element **11**, implemented with the basic elements **41, 43** and **45**, is larger than the measuring element **10**, in this example more particularly

$$C_{H,O} = 1.5 C_{M,O}$$

In the chosen example associated herewith

$$\frac{R_2}{R_1} = 1.02\,\frac{C_{M,O}}{C_{H,O}} = \frac{1.02}{1.5} = 0.68.$$

This value can be realized by means of a series arrangement of two precision resistors or with a co-integrated resistor in an integrated circuit having a tap at the 0.405^{th} portion of the length for which it holds that

$$\frac{0.405}{1 - 0.405} = 0.68.$$

Also here it holds that the manufacturing tolerances have a negligible influence on this ratio, although the absolute values of R_1 and R_2 will not be equal for all the produced items.

The electrodes indicated by means of a solid line can be provided with dummy projections **51** to **55**, inclusive, located opposite the connecting conductors. These projections ensure that a slight relative shift between the first and the second cover plate occurring during assembly of the display screen does not affect the capacitance of the basic element so that also this manufacturing tolerance does not influence the control accuracy. The effect of a slight horizontal shift is also negligible owing to a sufficient overlapping by the counter electrode **46**.

It is obvious that the element need not be exactly aligned, as shown in FIG. **5**, but that they may be distributed in an apparently random manner over the display screen, thus that both C_H and C_M furnish the best possible approximation of the chosen values if the thickness of the display screen would vary somewhat into the horizontal and/or the vertical direction.

Finally, it should be noted that a high multiplex factor can also be achieved by means of the known two frequency control, which, however, usually requires

high drive voltage. Such a display apparatus can also be fruitfully implemented in accordance with the invention; so that either lower voltages will be sufficient, or a still higher multiplex factor can be realised at the same voltages.

What is claimed is:

1. A display device comprising

a display screen having a plurality of display elements and a measuring element, said display screen comprising a liquid crystal enclosed between a first and a second cover plate each having a plurality of excitation electrodes for applying electric display drive voltages to said display elements and for applying an electric measuring device voltage to said measuring element;

an excitation circuit for generating said display drive voltages and said measuring drive voltage;

a control circuit having at least a measuring input for an electric measuring signal, said measuring input being coupled to one of said excitation electrodes of said measuring element, and at least a control output for an electric control signal,

said control circuit adjusting amplitudes of said display drive voltages and of said measuring drive voltage to a value corresponding to the threshold voltage of the liquid crystal in response to impedance variations of said measuring element resulting from temperature and voltage dependence of said liquid crystal,

characterized in that said display screen also comprises an auxiliary measuring element which differs in size from said measuring element, said auxiliary measuring element being arranged in series with said measuring element, said series arrangement having ends coupled to said excitation circuit for supplying said measuring drive voltage, and the junction of the measuring element and the auxiliary measuring element being coupled to said measuring input of said control circuit.

2. A display device as claimed in claim 1, characterized in that said control circuit comprises

a differential amplifier, a first and a second signal input which constitute a first and a second measuring input of said control circuit; and

a further series arrangement of a first and a second bridge impedance, ends of said further series arrangement being connected to ends of said series arrangement of said measuring element and said auxiliary measuring element for forming a bridge circuit,

wherein the junction of said measuring element and said auxiliary measuring element is coupled to the first measuring input and the junction of the first and the second bridge impedance is coupled to the second measuring input.

3. A display device as claimed in claim 2, characterized in that said first and second bridge impedances are resistors.

4. A display device as claimed in claim 1, characterized in that

said control circuit comprises a differential amplifier, a first and a second signal input which constitute a first and a second measuring input of said control circuit; and

said excitation circuit comprises a series arrangement of a first and a second electric voltage source for producing said measuring drive voltage;

wherein said junction of said measuring element and said auxiliary measuring element is coupled to said first measuring input and the junction of said first and second voltage source is coupled to said second measuring input.

5. A display device as claimed in any one of the preceding claims, characterized in that said measuring element and said auxiliary measuring element are formed from a plurality of equal and identical basic elements.

6. A display device as claimed in claim 5, characterized in that said basic elements are evenly distributed over said display screen.

7. A display device as claimed in claim 1, characterized in that said excitation circuit is of a type wherein amplitudes of said drive voltages generated by said excitation circuit are predominantly proportional to a supply voltage applied to said excitation circuit, a supply input of said excitation circuit being connected to a supply output of a controllable power supply having a control input for an electric control signal, said control input being coupled to said control output of said control circuit.

* * * * *

APPENDIX G

***Okabe* Reference**

U.S. Patent No. 5,940,184

US005940184A

United States Patent [19]

Okabe

[11] Patent Number: 5,940,184

[45] Date of Patent: Aug. 17, 1999

[54] PHOTOGRAPHING METHOD AND APPARATUS USING A PHOTOCONDUCTIVE LAYER FORMED ON AN ELECTRODE AND A LIQUID CRYSTAL POLYMER COMPOSITE

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[52] U.S. Cl. 358/296; 347/238

[58] Field of Search 358/296, 302, 358/335, 345; 347/233, 238; 348/38, 50, 87; 359/36, 55

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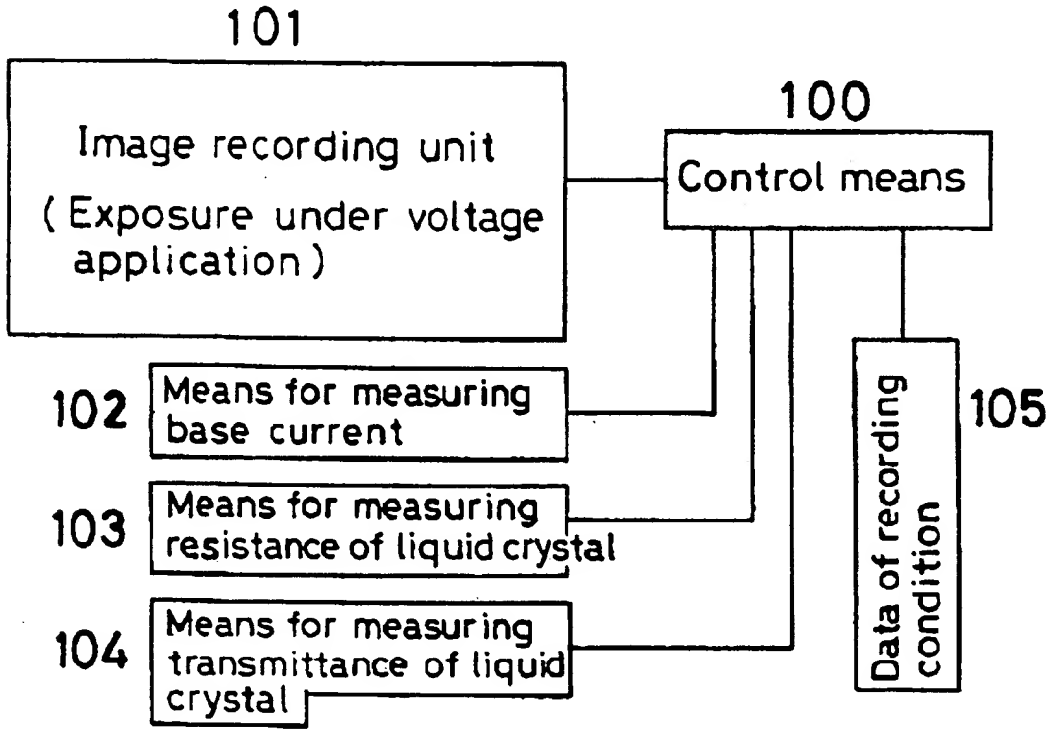
[57] ABSTRACT

A photographic method for controlling characteristics of an image to be recorded by changing the conditions for voltage application and achieves image recording by setting application voltage in accordance with image characteristics as desired. The range of external application voltage is set according to resistance of the liquid crystal medium, threshold voltage of the liquid crystal medium, and base current of a photo sensor, and the application voltage is changed according to the desired image characteristics within the preset range.

3 Claims, 11 Drawing Sheets



PRIOR ART

FIG. 1

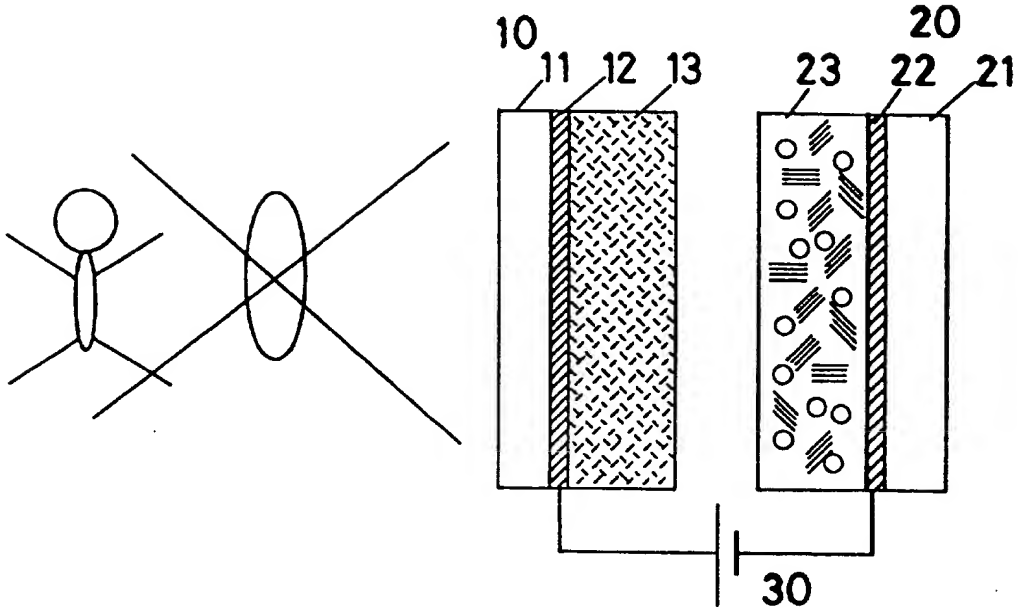


FIG. 2 (a)

PRIOR ART

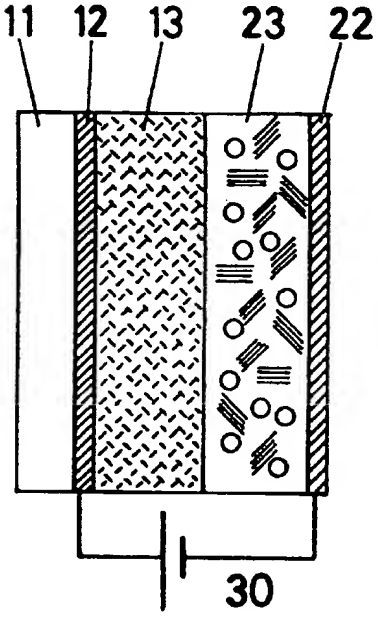


FIG. 2 (b)

PRIOR ART

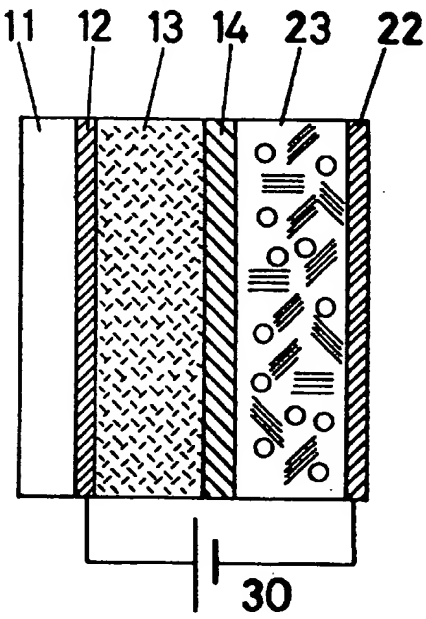


FIG. 3
PRIOR ART

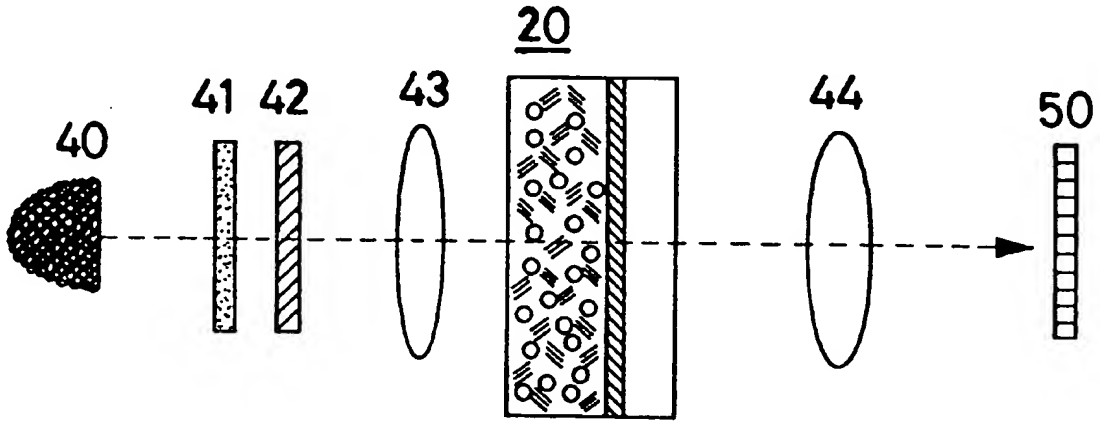


FIG. 4

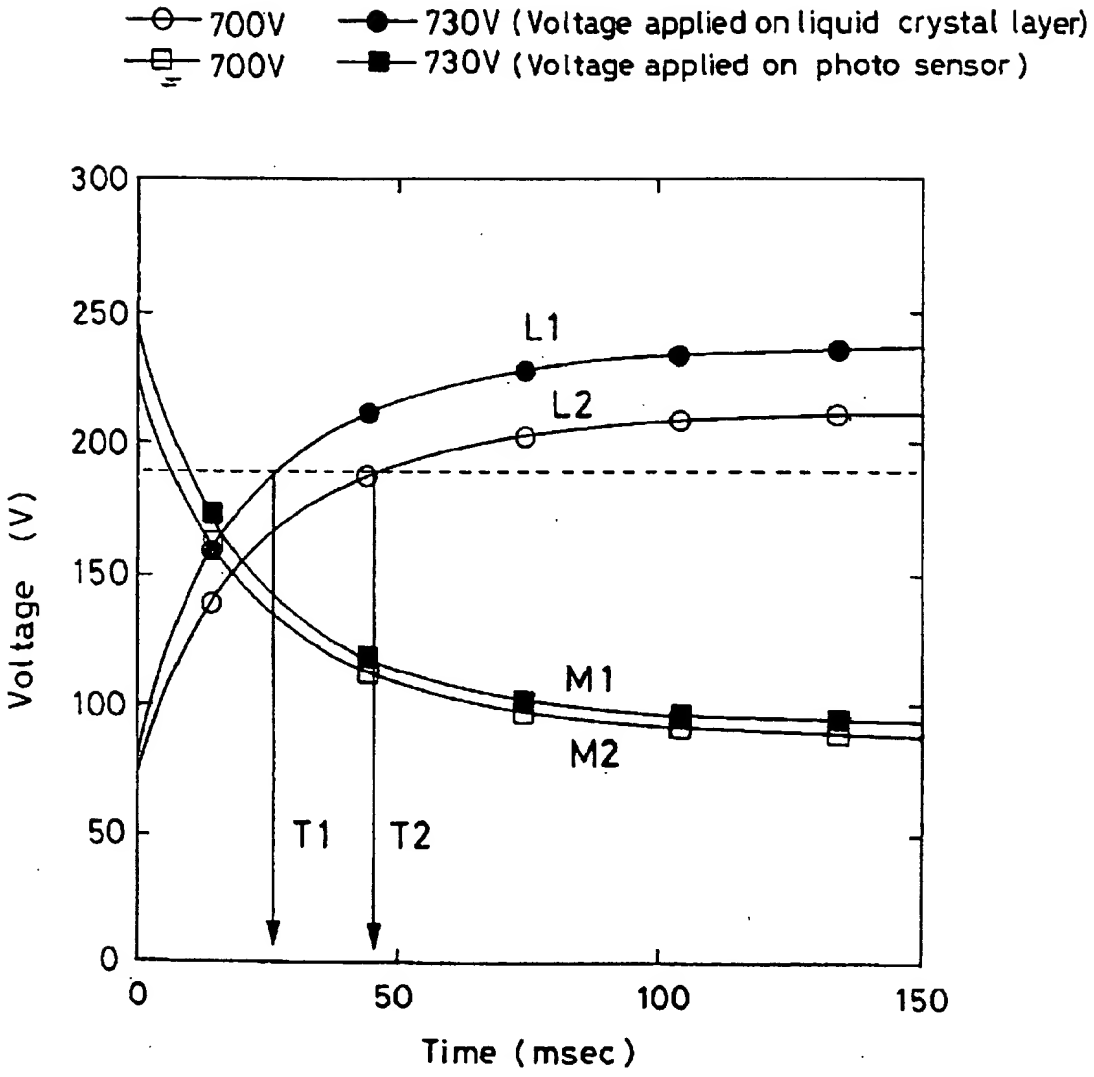

700V
730V (Voltage applied on liquid crystal layer)
700V
730V (Voltage applied on photo sensor)
300
250
200
150
100
50
0
Voltage (V)
L1
L2
M1
M2
T1
T2
0
50
100
150
Time (msec)

FIG. 5

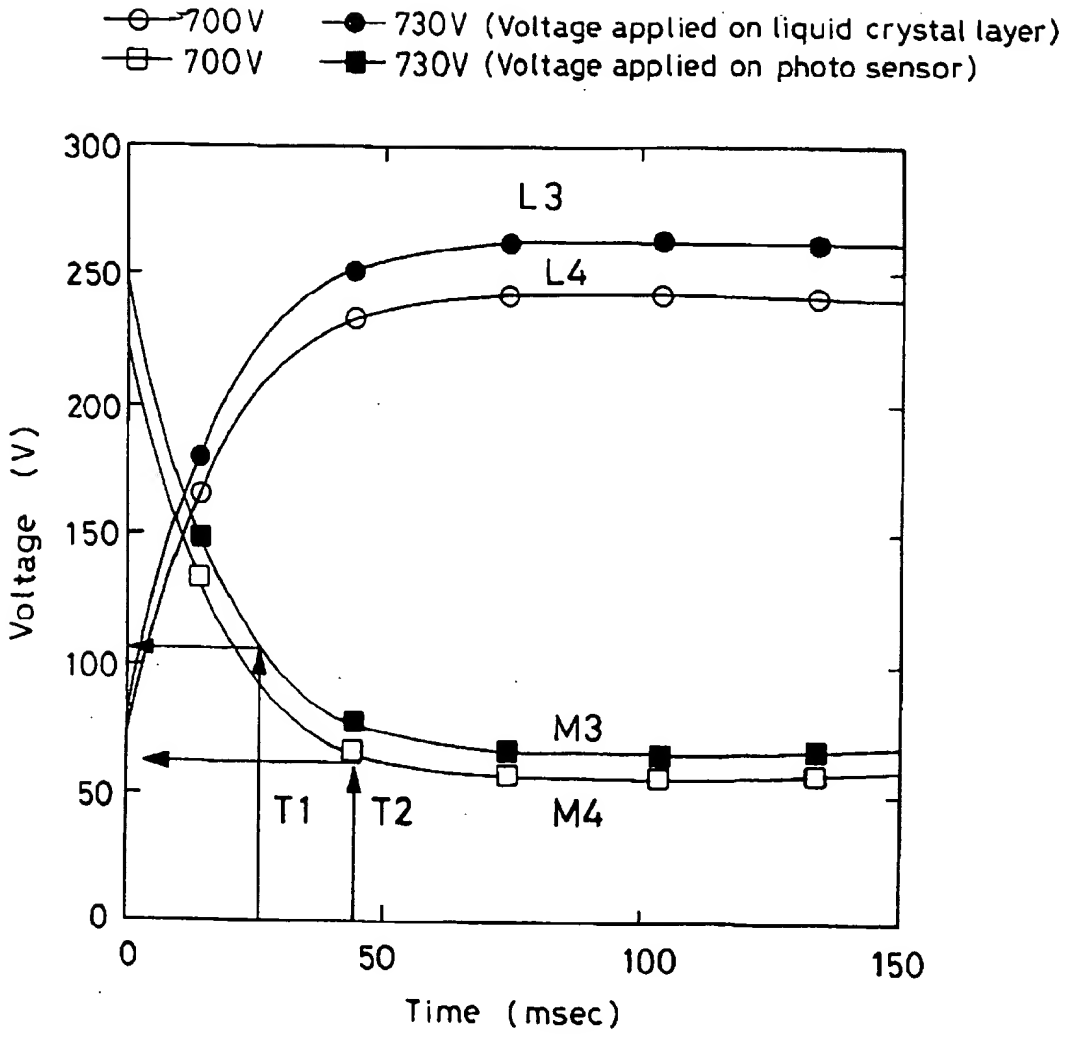
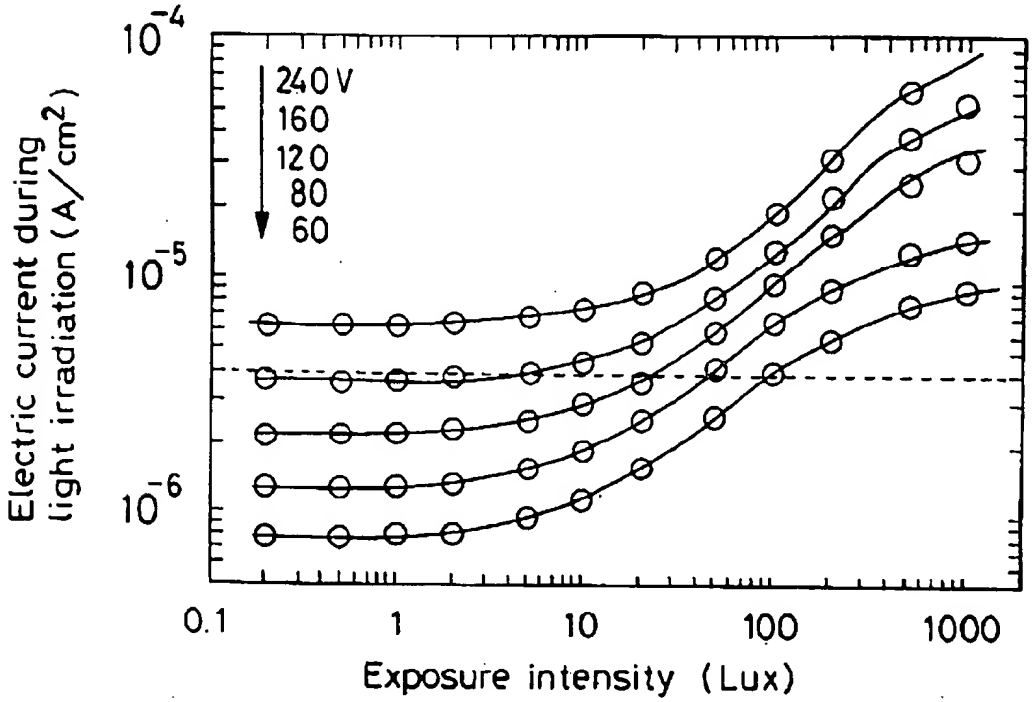

700V
730V (Voltage applied on liquid crystal layer)
700V
730V (Voltage applied on photo sensor)
300
250
200
150
100
50
0
Voltage (V)
L3
L4
M3
M4
T1
T2
0
50
100
150
Time (msec)

FIG. 6



Electric current value 33 msec after starting of light irradiation

FIG. 7

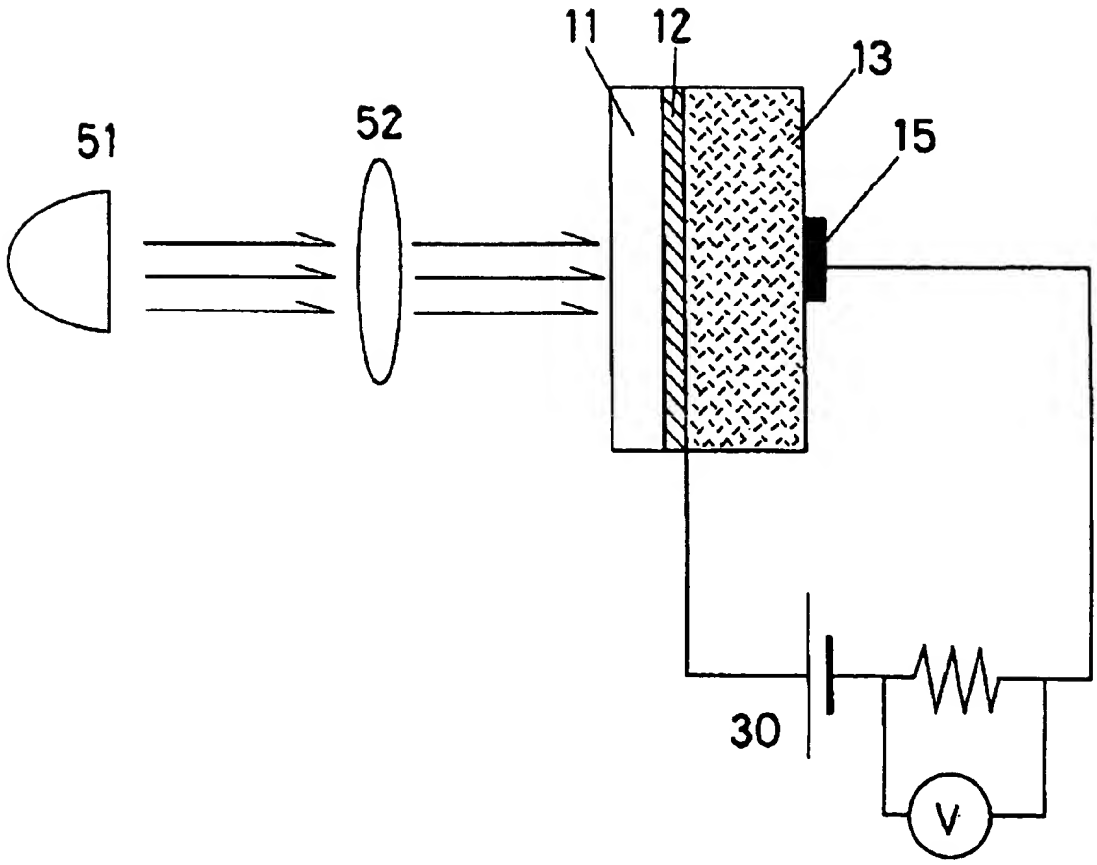


FIG. 8

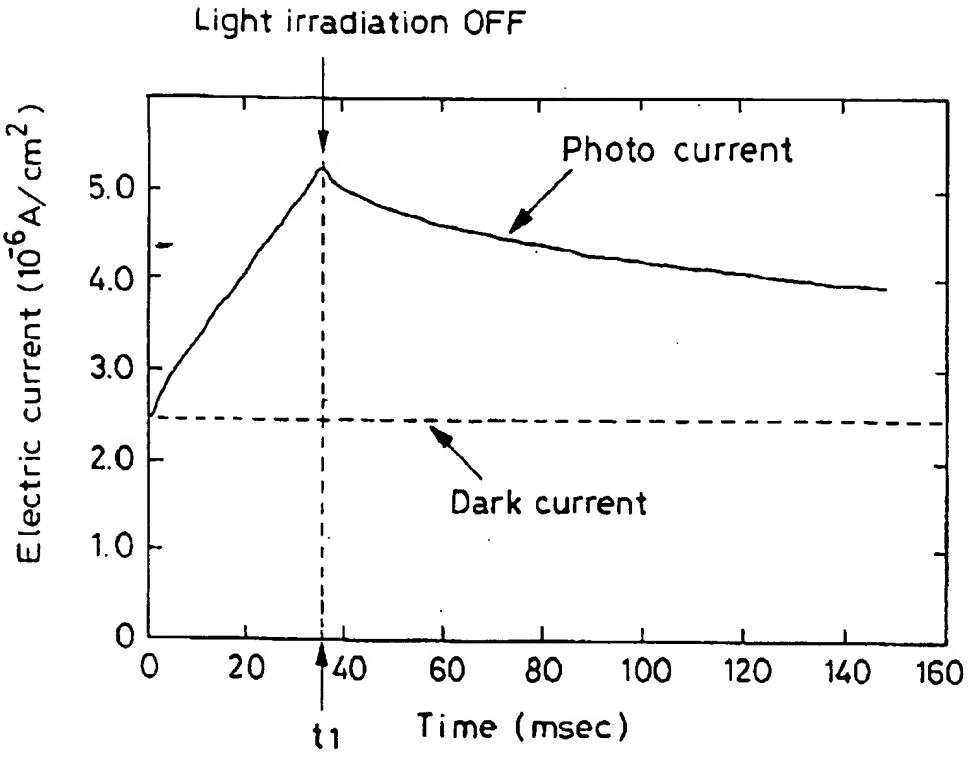

Light irradiation OFF
Photo current
Dark current
Electric current (10^{-6}A/cm^2)
5.0
4.0
3.0
2.0
1.0
0
0
20
40
60
80
100
120
140
160
t1
Time (msec)

FIG. 9

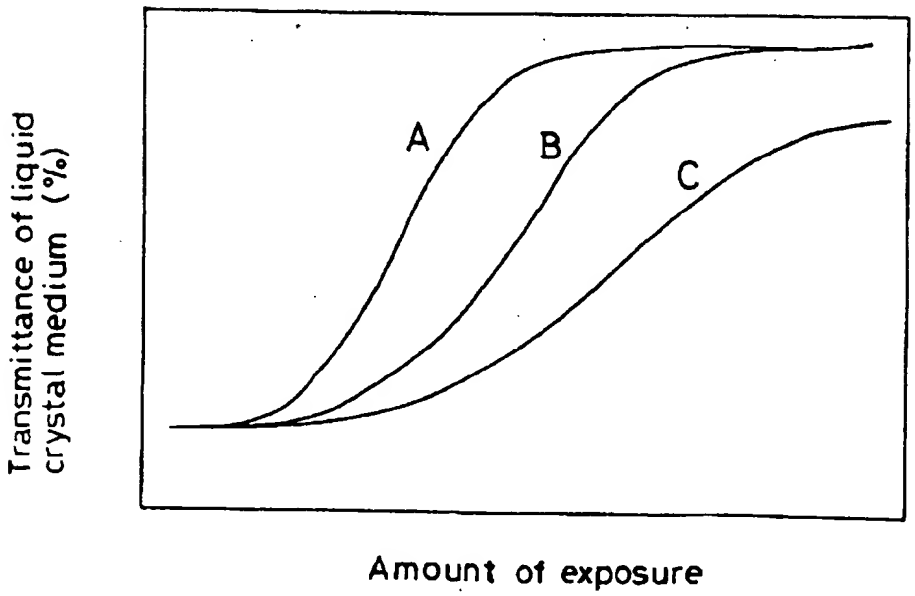

A
B
C
Transmittance of liquid crystal medium (%)
Amount of exposure

FIG. 10

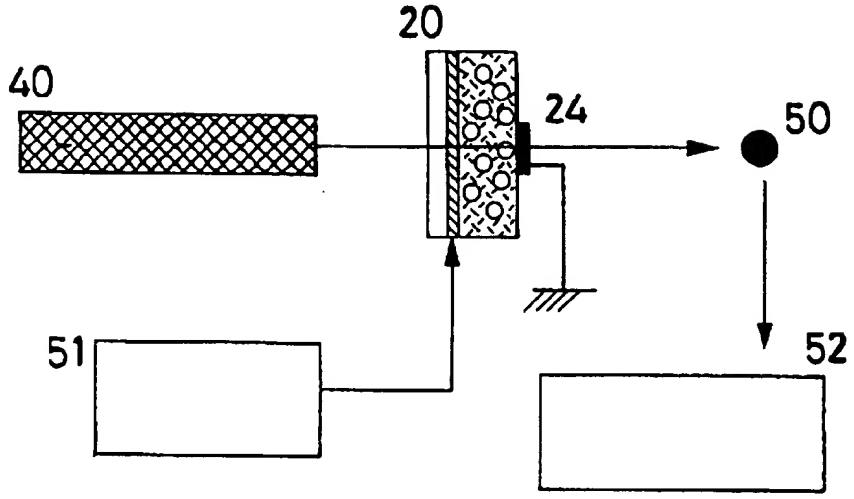

20
40
24
50
51
52

FIG. 11

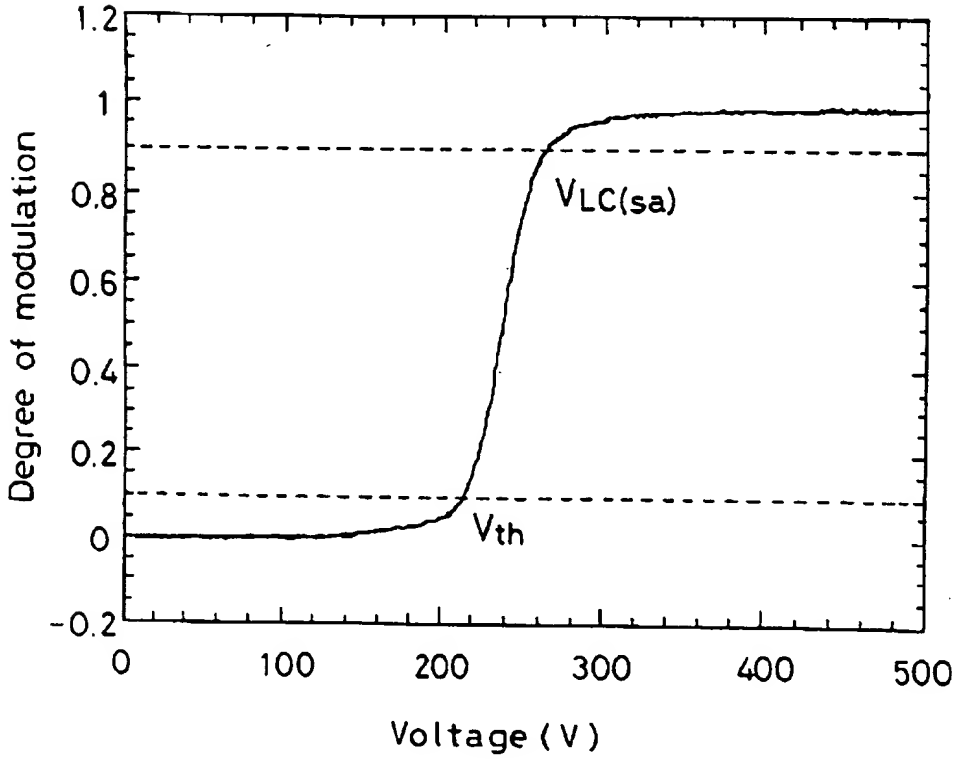

1.2
1
0.8
0.6
0.4
0.2
0
-0.2
Degree of modulation
VLC(sa)
Vth
0
100
200
300
400
500
Voltage (V)

FIG. 12

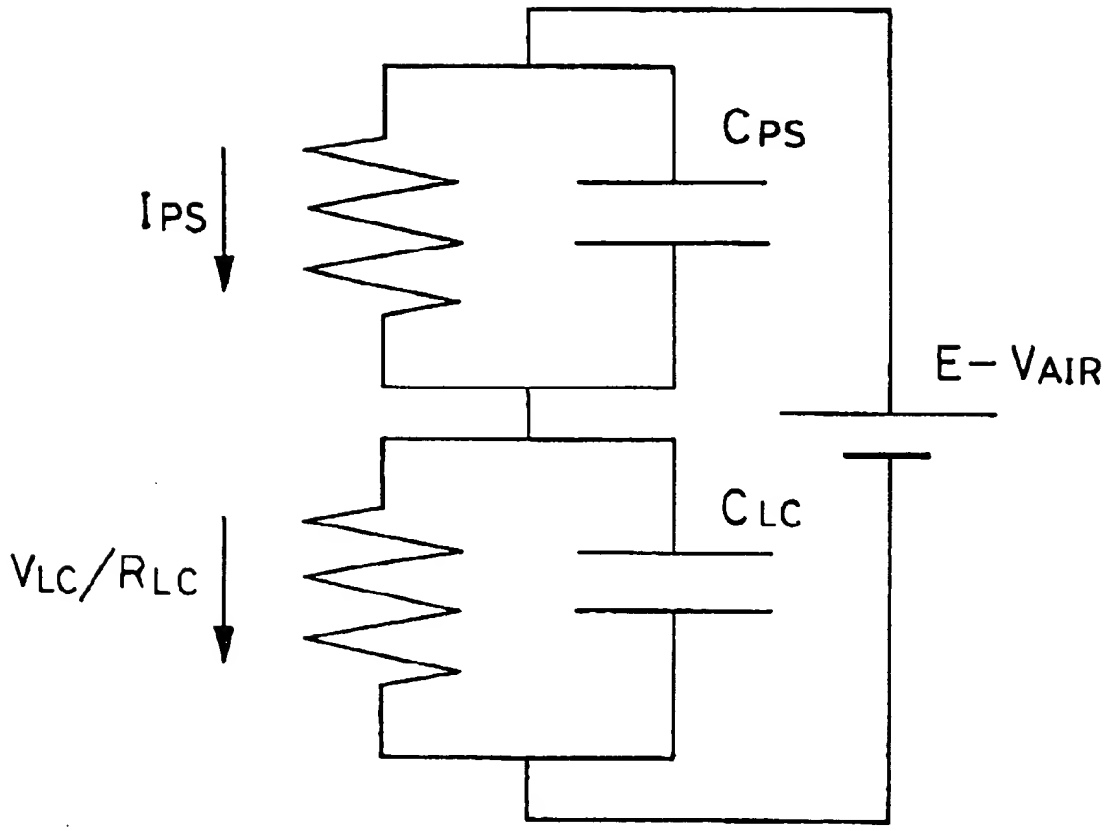


FIG. 13

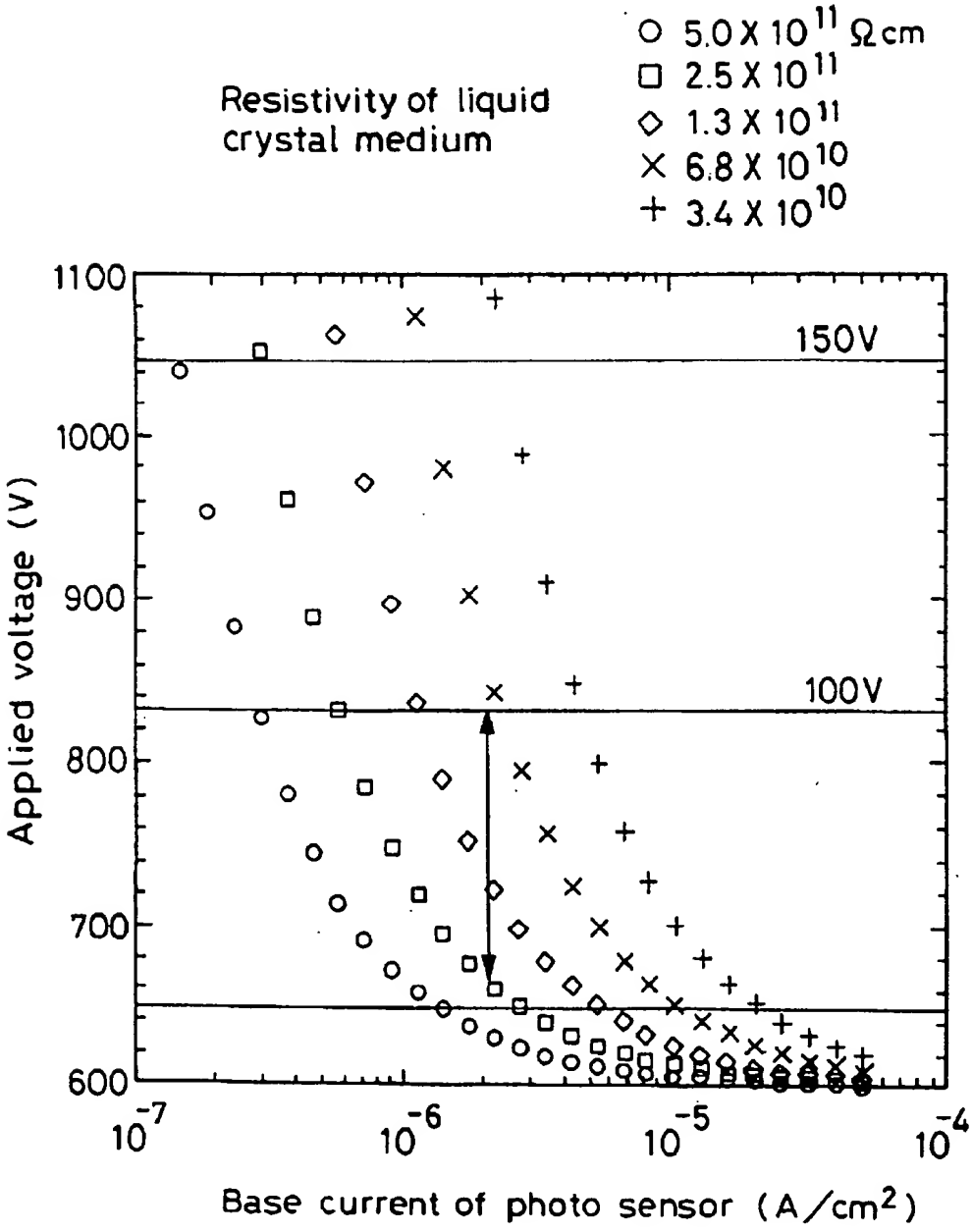

Resistivity of liquid crystal medium
○ 5.0 X 10^11 Ωcm
□ 2.5 X 10^11
◇ 1.3 X 10^11
× 6.8 X 10^10
+ 3.4 X 10^10
150V
100V
Applied voltage (V)
1100
1000
900
800
700
600
10^-7
10^-6
10^-5
10^-4
Base current of photo sensor (A/cm^2)

FIG. 14

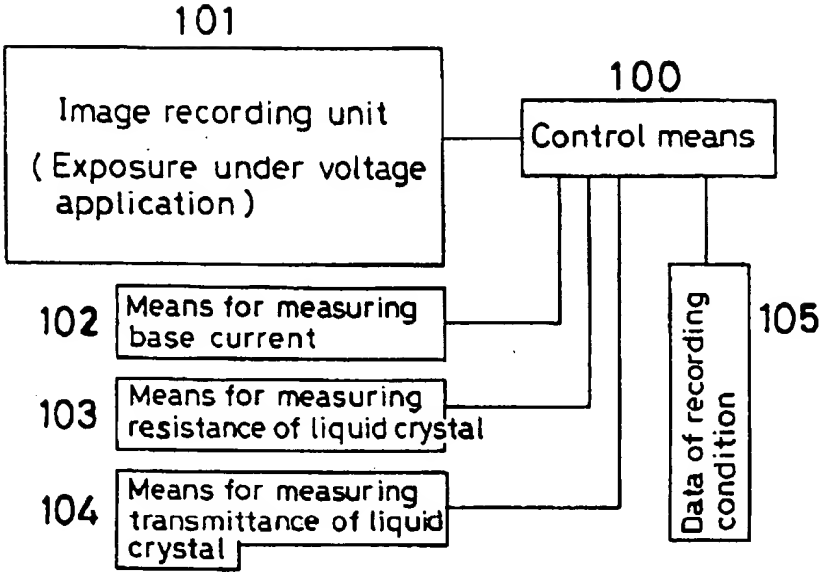
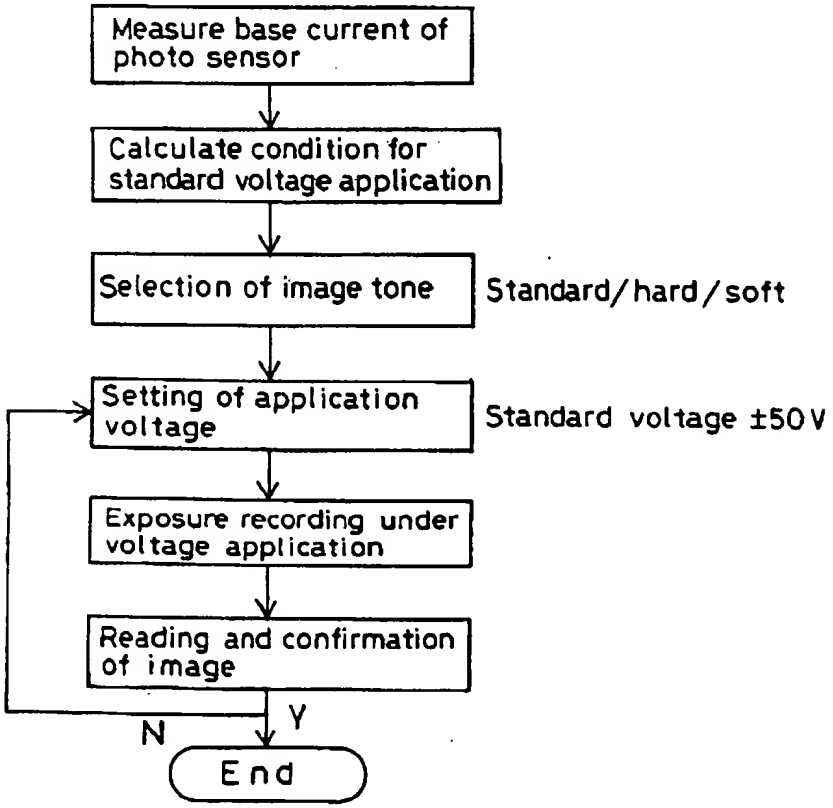

101
Image recording unit
(Exposure under voltage application)
100
Control means
102
Means for measuring base current
103
Means for measuring resistance of liquid crystal
104
Means for measuring transmittance of liquid crystal
Data of recording condition
105

FIG. 15


Measure base current of photo sensor
Calculate condition for standard voltage application
Selection of image tone
Standard/hard/soft
Setting of application voltage
Standard voltage ±50V
Exposure recording under voltage application
Reading and confirmation of image
N
Y
End

PHOTOGRAPHING METHOD AND APPARATUS USING A PHOTOCONDUCTIVE LAYER FORMED ON AN ELECTRODE AND A LIQUID CRYSTAL POLYMER COMPOSITE

BACKGROUND OF THE INVENTION

The present invention relates to a photographing method and a photographing apparatus using a photo sensor having a photoconductive layer formed on an electrode and a liquid crystal polymer composite, where liquid crystal is dispersed and fixed in resin.

It is known that a liquid crystal polymer composite can be prepared by mixing liquid crystal with resin and by dissolving it in a common solvent, and after this solution is coated by a spinner, the solvent is evaporated and dried, and the liquid crystal phase and the resin phase are separated by phase separation. The liquid crystal polymer composite can also be prepared by dissolving liquid crystal and monomer or oligomer of UV-setting resin in a common solvent, and under the condition where the mixture of the liquid crystal and the monomer is dried at a temperature to form an isotropic phase, ultraviolet ray is irradiated to polymerize the monomer, and the resin phase and the liquid crystal phase are separated by phase separation.

In the phase separation of the liquid crystal phase and the resin phase, liquid crystal phase in spherical or other shape is dispersed in the resin in some cases, or resin balls are dispersed in the liquid crystal phase with a skin layer on the surface in some other cases.

Refractive index in the orienting direction of the liquid crystal phase is adjusted in such manner that it becomes approximately equal to the refractive index of the resin. Because the refractive index in the non-oriented status is different from the refractive index of the resin, light is scattered at interface between the liquid crystal phase and the resin under a non-oriented condition immediately after preparation of the liquid crystal medium, and transmittance of the medium is decreased. When electric field is applied on the liquid crystal medium and the liquid crystal is oriented in a direction perpendicular to the plane of the medium, scattering is eliminated, and the light is transmitted.

If smectic liquid crystal having memory property is used as the liquid crystal, even when electic field is applied to orient the liquid crystal and electric field is then removed, the oriented status is maintained. When it is heated to a temperature where the liquid crystal phase is turned to isotropic phase and is then cooled down, it can be restored to the non-oriented status.

To record an image information on the liquid crystal medium, a transparent electrode **22** and a liquid crystal polymer composite layer **23** are sequentially formed on a transparent support member **21** to prepare a liquid crystal recording medium **20**, and a transparent electrode **12** and a photoconductive layer **13** are sequentially formed on a transparent support member **11** to prepare a photo sensor **10** as shown in FIG. **1**. The liquid crystal recording medium **20** and the photo sensor **10** are placed at face-to-face position with an air gap between them. Then, voltage is applied from a power source **30** between the two electrodes, and image exposure is performed on the photo sensor **10**. The electric field on the liquid crystal is changed according to intensity of the exposure. Liquid crystal is oriented according to the electric field, and an image information corresponding to the image exposure can be recorded.

There is another method to record an image on a liquid crystal recording medium using a photo sensor: As shown in FIG. **2**(*a*), a transparent electrode **12**, a photoconductive layer **13**, a liquid crystal polymer composite layer **23**, and an upper electrode **22** are sequentially formed on a transparent support member **11** to prepare an integrated type recording medium. Or, as shown in FIG. **2**(*b*), a transparent electrode **12**, a photoconductive layer **13**, a dielectric intermediate layer **14**, a liquid crystal polymer composite layer **23**, and an upper electrode **22** are sequentially laminated to prepare an integrated type recording medium. Image exposure is performed with the photo sensor by the same procedure, and by applying voltage between the two electrodes from the power source **30**, an image information can be recorded on the liquid crystal layer.

The image information recorded on the liquid crystal medium can be converted to electric signal by an image reading device as shown in FIG. **3**. In FIG. **3**, illumination light with adequate wavelength selected in an optical system comprising a light source **40**, an IR cut filter **41**, a band-pass filter **42**, and an illumination lens **43** is irradiated to a liquid crystal recording medium **20**. The light passing through in the liquid crystal medium is adjusted in such manner that an image is formed on a CCD line sensor **50** through an image forming lens **44**. The liquid crystal recording medium is placed on a movable stage (not shown), and said stage is controlled by a stepping motor. By converting the transmitted light by a CCD sensor to electric signal as the stage is moved, the image information is read.

The image signal converted to electric signal is outputted to a CRT or a printer when necessary.

In case it is attempted to record an image by the exposure under voltage application as described above, satisfactory image may not be obtained unless the image is recorded under adequate voltage application. Also, because the characteristics of the image to be recorded are changed according to the application voltage, an image of the desired characteristics may not be recorded unless correlation between the application voltage and the characteristics of the image to be recorded are well identifed.

To solve the above problems, it is an object of the present invention to provide a photographing method and a photographing apparatus, by which it is possible to control the recording characteristics of an image to be recorded by changing voltage applying conditions and to record the image by setting the application voltage to match the desired characteristics of the image.

To attain the above object, the method for recording image information according to the present invention comprises a photo sensor having a photoconductive layer formed on a transparent electrode and a liquid crystal recording medium having a liquid crystal polymer composite layer consisting of resin and liquid crystal formed on an electrode, said photo sensor and said liquid crystal recording medium placed face-to-face with an air gap therebetween to form a separate type information recording medium, image exposure is performed to the photo sensor, said liquid crystal is oriented by applying voltage between the two electrodes, and image information is recorded, whereby an application voltage, at which initial distribution voltage to the liquid crystal medium determined by capacities of the liquid crystal medium and the photo sensor is ½ or less of threshold voltage of the liquid crystal medium, is defined as an upper limit application voltage, a sum V1 of saturation voltage of the liquid crystal medium and breakdown voltage, or an application voltage V2 where equilibrium potential of the liquid crystal medium obtained from resistance of the photo sensor based on base current of the photo sensor and from

resistance of the liquid crystal medium is higher than the threshold voltage, whichever is higher, is defined as a lower limit application voltage, and an image is recorded by setting the application voltage between the upper limit application voltage and the lower limit application voltage.

The present invention is characterized in that image characteristics are controlled by changing the application voltage within the preset range.

Also, the apparatus for recording image information according to the present invention comprises a photo sensor having a photoconductive layer formed on a transparent electrode and a liquid crystal recording medium having a liquid crystal polymer composite layer consisting of resin and liquid crystal formed on an electrode, said photo sensor and said liquid crystal recording medium placed face-to-face with an air gap therebetween to form a separate type information recording medium, image exposure is performed to the photo sensor, said liquid crystal is oriented by applying voltage between the two electrodes, and image information is recorded, whereby there are provided means for measuring resistance of the liquid crystal medium, means for determining base current of the photo sensor, and control means for setting application voltage range, said control means calculates an upper limit application voltage, defined as the voltage, at which initial distribution voltage to the liquid crystal medium determined by capacities of the liquid crystal medium and the photo sensor is ½ or less of the threshold voltage of the liquid crystal medium, and also calculates a lower limit application voltage as a sum V1 of saturation voltage of the liquid crystal medium and breakdown voltage, or an application voltage V2 where equilibrium potential of the liquid crystal medium obtained from resistance of the photo sensor based on base current of the photo sensor and from resistance of the liquid crystal medium is higher than the threshold voltage, whichever is higher, and the application voltage is controlled within the range of said upper limit application voltage and said lower limit application voltage.

According to the present invention, the range of the external application voltage is set at least based on the resistance of the liquid crystal, threshold voltage of the liquid crystal medium, and base current of the photo sensor, and by changing the application voltage in accordance with the desired image characteristics within the preset range, photographing can be achieved with the desired image characteristics.

Further, it is preferable to provide a coating layer on the surface of the fired porous ceramic molded material.

Still other objects and advantages of the invention will in part be obvious and will in part be apparent from the specification.

The invention accordingly comprises the features of construction, combinations of elements, and arrangement of parts which will be exemplified in the construction hereinafter set forth, and the scope of the invention will be indicated in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 represents an illutration showing a method for recording an image on a separate type liquid crystal medium;

FIGS. 2(*a*) and 2(*b*) represent drawings for explaining a method for recording an image on an integrated type liquid crystal medium;

FIG. 3 is a drawing of a method for reading an image;

FIG. 4 is a diagram showing change of voltage applied to the liquid crystal medium and the photo sensor on a non-exposed portion;

FIG. 5 is a diagram showing change of voltage applied to the liquid crystal medium and the photo sensor on an exposed portion;

FIG. 6 is a diagram showing relationship between exposure intensity and value of photo sensor current;

FIG. 7 is a drawing for explaining a method for measuring photo sensor current;

FIG. 8 is a diagram showing change of current value of the photo sensor;

FIG. 9 represents a diagram showing relationship between amount of exposure and transmittance of the liquid crystal medium;

FIG. 10 is a schematical drawing of an apparatus for measuring threshold voltage and saturation voltage;

FIG. 11 is a diagram showing the results of the measurement;

FIG. 12 is a circuit diagram showing an equivalent circuit of a separate type liquid crystal recording medium;

FIG. 13 is a diagram for explaining a method for setting the condition for voltage application;

FIG. 14 shows an arrangement of a photographing apparatus; and

FIG. 15 represents a flow chart for setting application voltage.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

First, description will be given on a method for applying voltage according to the present invention.

FIG. 4 and FIG. 5 each represents the results of simulation to simulate the change over time of the voltage applied to a liquid crystal medium and a photo sensor.

Physical property values used in the simulation are as follows:

Liquid crystal medium: Film thickness 6 μm; Resistivity 2.7×10^{11} $\Omega\cdot cm_j$

Photo sensor: Film thickness 10 μm; Base current 1.7×10^{-6} A/cm^2

(Base current: the current flowing when voltage of 100 V is applied under non-exposure condition) FIG. 4 shows the change over time of the voltage on the non-exposed portion, and FIG. 5 represents the change over time of the voltage on the exposed portion. In FIG. 4, L1 and L2 each represents the change over time of the voltage of the liquid crystal medium at the application voltage of 730 V and 700 V respectively, and M1 and M2 each represents the change over time of the voltage applied on the photo sensor at the application voltage of 730 V and 700 V respectively.

If it is assumed that threshold voltage of the liquid crystal medium (voltage where the liquid crystal medium is oriented) is 180 V in the system of the present invention, voltage is stopped when the voltage applied to the liquid crystal medium reaches the threshold voltage on the non-exposed portion. Before it reaches the threshold voltage, orientation of the liquid crystal is not sufficient, and necessary contrast cannot be obtained. If it is over the threshold voltage, the non-exposed portion is oriented, and image quality is reduced. In FIG. 4, the threshold voltage is reached at the time T1 (about 30 msec) in case the application voltage is 730 V and at the time T2 (about 45 msec) in case it is 700 V, and the voltage application is stopped.

FIG. 5 shows the change of voltage on the exposed portion, where L3 and L4 represent the change over time of the voltage applied on the liquid crystal medium when the application voltage is 700 V and 730 V respectively, and M3 and M4 represent the change over time of the voltage applied to the photo sensor when the application voltage is 700 V and 730 V respectively. In the simulation, the amount of the light to be irradiated is changed to match the change of the application voltage, and it is adjusted in such manner that the potential differences (contrast) of a bright portion and a dark portion are equal to each other when the voltage on the non-exposed portion reaches the threshold voltage. Here, the amount of exposure on the exposed portion is adjusted so that the voltage on the exposed portion is about 230 V when the voltage on the non-exposed portion reaches 180 V.

Taking notice of the voltage, which is applied on the photo sensor when the voltage application is stopped, it is about 60 V (the voltage at the time T2) in case the application voltage is 700 V, while it is about 105 V (voltage at the time T2) when the application voltage is 730 V.

FIG. 6 shows the relationship between the current when light is irradiated on the photo sensor (sum of photoelectric current and base curent) and intensity of the irradiated light.

The current flowing in the photo sensor can be measured, for example, as shown in FIG. 7, by arranging a gold electrode **15** on the surface of the photo sensor and by applying voltage between this and the transparent electrode **12** from the power source **30**. In this case, the results of the measurement when light of a given intensity is irradiated for a given period of time from the direction of the transparent electrode of the photo sensor using the light source **51** and the optical shutter **52** are as shown in FIG. **8**.

To the photo sensor, light was irradiated for 33 msec with a given voltage applied. As the time given on abscissa in the graph, the time when light irradiation was started was set to: t=0. Also, it was assumed that the current value when t=0 was dark current (base current) value, and current value in the graph is shown by the value per unit area (1 cm^2). After the light irradiation was started, the current value increased as time elapsed, and it gradually attenuated after the completion of light irradiation. In this way, photoelectric current continues to change during voltage application. In case light irradiation time is 33 msec, photoelectric current reaches the maximum after 33 msec and it gradually attenuates after the completion of light irradiation. Thus, photoelectric current is incessantly changing and is not constant. Hereinafter, it is supposed that the value of photoelectric current when t=33 msec (when the voltage application is stopped) is the photoelectric current value. The photoelectric current is dependent on light intensity of the irradiated light, and it increases as the intensity increases.

In the meantime, the value of the current flowing to the photo sensor as necessary for orienting the liquid crystal medium is determined by resistance and capacity of the liquid crystal medium. For example, if it is supposed to be $4\times10^{-6}A/cm^2$ as shown by the curves in FIG. **6**, irradiation intensity of about 80 lux is required when the voltage at the stopping of voltage application is 60 V, while the above current value can be obtained at about 20 lux in case the voltage at the stopping of the voltage application is 105 V. The current value during light irradiation is also dependent upon the time from the starting of light irradiation. To obtain the same current value, it is necessary to expose more to light when voltage is low. For this reason, by changing the application voltage, the voltage on the photo sensor at the stopping of voltage application is changed. The amount of exposure necessary to orient the liquid crystal is changed, and this leads to the change of the characteristics of the image to be recorded.

FIG. **9** shows transmittance characteristics of the liquid crystal to the amount of exposure when the application voltage is changed. The characteristics A are the highest, and next follow the chracteristics B and C in this order. In the characteristics A, latitude is narrow and this is suitable for the image such as characters, and the characteristics B are suitable for scenery image. By selecting the application voltage, soft image or hard image can be chosen according to each purpose. In the characteristics C, the application voltage is too low, and it does not reach saturation voltage (not sufficiently oriented). Therefore, S/N ratio is poor and it is not suitable for the purpose. In this way, by changing the application voltage, it is possible to control the characteristics of the image to be recorded (latitude) to suit each purpose.

Next, description will be given on a method for setting the application voltage.

First, description is given on threshold voltage and saturation voltage when the application voltage is set.

FIG. **10** is a block diagram of an apparatus for determining orientation status (transmittance of the liquid crystal by changing the voltage applied to the liquid crystal medium. A gold electrode (semitransparent) **24** is attached on the surface of the liquid crystal medium, and voltage is applied between the transparent electrode **22** and the gold electrode **24** using a voltage generator **51**. By irradiating laser beam from an argon laser (448 nm) **40**, the transmitted light is detected by a sensor **50**, and the detection result is monitored using an oscilloscope **52**.

The results of the measurement are as shown in FIG. **11**. In FIG. **11**, voltage is represented on the abscissa and degree of modulation is represented on the ordinate. These are defined by the following equation:

$$\text{Degree of modulation}=(T-Toff)/(Ton-Toff)$$

where

Ton: Signal value in oriented status

Toff: Signal value in non-oriented status

It is now supposed that, when the measurement results are standardized as described above, the voltage V_{th} of the liquid crystal medium when the degree of modulation is 0.1 is threshold voltage, and the voltage $V_{LC(as)}$ of the liquid crystal medium when the degree of modulation is 0.9 is saturation voltage.

In the image recording system of the present invention, the photo sensor or the liquid crystal medium is considered as a parallel circuit of resistance or capacitor respectively, and each of the se is represented by an equivalent circuit which comprises series circuit as shown in FIG. **12**.

As shown in the figure, it is supposed that capacities of the photo sensor and the liquid crystal recording medium are C_{PS} and C_{LC} respectively, that the voltage applied on both ends of the series circuit is V_{AP} (=supply voltage E−air gap voltage V_{AIR}), that voltage applied on the photo sensor and the liquid crystal recording medium are V_{PS} and V_{LS} respectively, and that the values of the current flowing in the photo sensor and the liquid crystal recording medium are I_{PS} and I_{LS} respectively, then:

$$V_{AP}=V_{PS}+V_{Air}+V_{LC} \quad (1),$$

where

V_{Air}: Breakdown voltage (Ex. 400 V)

It is supposed that the resistance of the photo sensor and the liquid crystal recording medium are R_{PS} and R_{LC}

respectively, and the voltage of the photo sensor and the voltage of the liquid crystal recording medium at dark portion under equilibrium condition at the elapse of sufficient time after voltage application are called equilibrium voltage and these are referred as $V_{PS(eq)}$ and $V_{LC(eq)}$ respectively. Then, the following relations exist:

$$V_{PS(eq)}/R_{PS}=V_{LC(eq)}/R_{LC} \quad (2)$$

$$R_{PS}=100/I_{PSd} \quad (3)$$

Here, I_{PSd} is base current value when voltage of 100 V is applied to the photo sensor. Also, the voltage $V_{LC}(0)$ distributed to the liquid crystal recording medium in initial stage is given by:

$$V_{LC}(0)=(V_{AP}-V_{Air})\cdot C_{PS}/(C_{PS}+C_{LC}) \quad (4)$$

With regard to the upper limit of the application voltage, if the initial distribution voltage $V_{LC}(0)$ given by the equation (4) is equal to or higher than the threshold voltage, in the system of the present invention, the liquid crystal is oriented before the exposure, and image recording cannot be achieved. If it is supposed that the threshold voltage is 200 V, for example, the initial distribution voltage V_{LC} (0) must be lower than 200 V, or preferably 150 V or lower, or most preferably ½ or less of the threshold voltage. In this way, the voltage distributed to the liquid crystal medium in the initial stage must be lower than the threshold voltage, or more preferably ½ or less of the threshold voltage, and this determines the upper limit of the application voltage.

Thus, the upper limit of the application voltage is determined by capacity and threshold voltage as shown in the equation (4), and it does not depend upon resistance or base current value and is constant. When threshold value increases, the upper limit of the application voltage naturally becomes higher. When the photo sensor becomes thicker, the capacity C_{PS} of the photo sensor decreases according to the equation (4), and the upper limit of V_{AP} increases.

Next, the lower limit of the application voltage is the two voltage values determined by the following two conditions, whichever is higher:

Condition (1): Sum of saturation voltage and breakdown voltage

For example, when breakdown voltage is 400 V and saturation voltage is 250 V, the lower limit application voltage is 650 V. When the liquid crystal medium reaches saturation voltage and is to be oriented completely, it is necessary to apply voltage, which is at least a sum of saturation voltage and breakdown voltage because the voltage of the photo sensor is 0 or lower in this case. Specifically, if the voltage applied on the photo sensor is 0, no current flows, and it is necessary to apply the above voltage or higher even at the lowest.

Condition (2): The minimum voltage required in order that the voltage of the liquid crystal medium on the non-exposed portion reaches threshold voltage

In a system where the liquid crystal medium and the photo sensor are placed face-to-face with an air gap therebetween and voltage is applied, when sufficient time elapses after voltage application, equilibrium status is reached at a voltage where the current on the photo sensor and the current on the liquid crystal medium at dark portion are equal to each other. The voltage values of the liquid crystal medium and the photo sensor in this case are expressed by the equation (2), and the equilibrium voltage $V_{LC(eq)}$ of the liquid crystal given by the equation (2) must be higher than the threshold voltage. Therefore, if $V_{LC(eq)}$ is obtained in the equation (2), the lower limit of the application voltage V_{AP} in this case is calculated from the equation (1) under the condition:

$$V_{LC(eq)} \geq V_{th},$$

then it is possible to obtain the lowest possible application voltage required, by which the voltage on the liquid crystal medium reaches the threshold voltage.

To obtain $V_{LC(eq)}$ in the equation (2), base current value of the photo sensor does not necessarily have linear characteristics to the voltage. Thus, the relationship between voltage and base current of the photo sensor is determined and is plotted, and $V_{LC(eq)}$ is calculated from the equation (2). Or, in case it is possible to approximate that the relationship between voltage and base current is linear, resistance value may be calculated in the equation (3) from the base current value at a given voltage (e.g. base current value at 100 V), and the above value may be obtained by the same procedure.

FIG. 13 shows how the relationship between the base current value when the application voltage is 100 V and the lower limit of the application voltage is calculated. The resistance of the liquid crystal medium has been calculated from resistivity and thickness of the medium. Resistance value of the liquid crystal medium (Ω/cm^2; Film thickness of the, liquid crystal is 6 nm.) is shown on the abscissa, and the application voltage V_{AP} (V) is given on the ordinate. FIG. 13 also shows the results (825 V and 1050 V) when the application voltage V.P is calculated in case the voltage V (0) distributed to the liquid crystal medium in initial stage is 100 V and 150 V respectively. In the figure, resistivity of the liquid crystal medium is given by symbols, where ○ represents 5.0×10^{11} Ωcm, □ represents 5×10^{11} Ωcm, ◇ represents 1.3×10^{11} Ωcm, X represents 6.8×10^{10} Ωcm, and+ represents 3.4×10^{10} Ωcm.

In FIG. 13, in case threshold voltage of the liquid crystal medium is 200 V, the application voltage, at which the voltage distributed in initial stage is ½ of threshold voltage, i.e. 100 V, is 830 V, and this value is the upper limit of the application voltage.

Taking an example in a case where base current of the photo sensor is $2\times10^{-6}A/cm^2$, resistivity of the liquid crystal medium is 2.5×10^{11} Ωcm (in case of □), the lower limit of the application voltage is about 680 V. When voltage lower than this is applied, the voltage of the liquid crystal medium on the non-exposed portion does not reach threshold voltage even when the time of voltage application is extended. Accordingly, the liquid crystal is not oriented, and a satisfactory image cannot be recorded. Therefore, in the case of this combination, the range of the application voltage suitable for image recording is between 630 V–830 V (the range shown by an arrow in the figure), and standard voltage applying condition is: 740 V to 750 V.

In case the same photo sensor is used, and if resistivity of the liquid crystal medium is 5.0×10^{11} Ωcm, the lower limit of the application voltage calculated from resistance value (the above condition (2)) is 630 V. In case an image is recorded at such applied voltage, the condition (2) is satisfied, and the voltage of the liquid crystal medium on the non-exposed portion reaches threshold voltage. Even when strong light is irradiated on the image exposed portion, saturation voltage of the liquid crystal medium cannot be reached, and it is not possible to completely orient the liquid crystal medium. This is not desirable.

When the same photo sensor is used, and if resistivity of the liquid crystal medium is 6.8×10^{10} Ωcm, the lower limit of the application voltage obtained from the condition (2) is higher than the upper limit of the applied voltage obtained from the initial distribution of voltage, and this combination is not suitable for image recording.

In case base current of the photo sensor is $2\times10^{-6}A/cm^2$ and resistivity of the liquid crystal medium is 2.5×10^{11} Ωcm,

it is known that the range of the adequate application voltage is 680 V to 830 V. In case the application voltage is 690 V, for example, the voltage applied to the photo sensor is 40 V if the voltage of the liquid crystal medium is saturation voltage, i.e. 250 V. To pass electric current necessary for completely orienting the liquid crystal medium at this voltage, it is necessary to expose the medium to considerably strong light. In case the application voltage is 730 V, voltage twice as high as the above is applied on the photo sensor, and the liquid crystal medium can be oriented by the light weaker than this.

In this way, in case the application voltage is closer to the lower limit of the condition, the voltage applied to the photo sensor becomes lower, and it is necessary to irradiate stronger light. As a result, the exposure range is widened.

As described above, the lower the application voltage is, the wider latitude is, i.e. soft image is obtained, and the higher the application voltage is, the narrower latitude is, i.e. hard image is obtained. Thus, by selecting the application voltage, it is possible to select soft or hard image.

In case resistance value of the liquid crystal medium, base current value of the photo sensor, threshold value and saturation voltage of the liquid crystal, and film thickness of liquid crystal medium and that of photo sensor are changed, the voltage can be set by the same procedure.

The base current value of the photo sensor can be measured immediately before image recording by the method shown in FIG. **7** in the image recording device. The resistance value of the liquid crystal recording medium may be measured in the image recording device similarly to the photo sensor.

The values measured in advance may be used as threshold voltage and saturation voltage of the liquid crystal, and film thickness of liquid crystal medium and that of photo sensor are changed, the voltage can be set by the same procedure.

The base current value of the photo sensor can be measured immediately before image recording by the method shown in FIG. **7** in the image recording device. The resistance value of the liquid crystal recording medium may be measured in the image recording device similarly to the photo sensor.

The values measured in advance may be used as threshold voltage and saturation voltage of the liquid crystal medium.

In the above, description has been given on the case of separate type liquid crystal recording medium. In case the liquid crystal medium and the photo sensor are directly formed on an integrated type liquid crystal recording medium as shown in FIG. **2**, the application voltage can be set by the same procedure as in the separate type liquid crystal recording medium by setting the breakdown voltage to 0. In-case a dielectric layer is placed between liquid crystal medium and photo sensor and is laminated, the voltage on the dielectric intermediate layer changes, and this is not necessarily the same as in the case of the separate type. If it is supposed that the dielectric intermediate layer consists of capacitor and resistance and if the change of voltage applied on it is taken into account, it is possible to set the application voltage by the same procedure.

Description is now given of an arrangement of a photographing apparatus and of a flow of photographing processing for setting the application voltage, referring to FIGS. **14** and **15**.

FIG. **14** shows an arrangement of a photographing apparatus of the present invention.

An image recording unit **101** comprises a separate type or an integrated type liquid crystal recording medium, a photographing optical system, a power source, a switch, etc. A base current measuring means **102** comprises, for example, a measuring device as explained in FIG. **7**. A liquid resistance measuring means **103** is arranged, for example, in such manner that an electrode is disposed on the liquid crystal medium, and by applying voltage between this electrode and the transparent electrode of the liquid crystal medium, the flowing current is measured. A liquid crystal transmittance measuring means **104** comprises an apparatus with an arrangement as shown in FIG. **10**. A control means **100** comprises a microcomputer and others and it is to incorporate a data **105** such as the measured base current, resistance of liquid crystal, or threshold value, saturation voltage, etc. of the liquid crystal measured in advance and stored, and also, it is to obtain the range of the applied voltage and to control the image recording unit. With regard to the image recording, transmittance of the non-exposed portion is monitored by the liquid crystal transmittance measuring means **104**, and voltage application is stopped when this reaches the predetermined value.

Next, description will be given of the flow of photographic processing, referring to FIG. **15**.

In the recording apparatus, voltage of 100 V is applied and base current of the photo sensor is measured. Next, using the equations (1) to (4), the lowest application voltage and the range of the application voltage are obtained, at which the initial distribution voltage of the liquid crystal medium is ½ or less of the threshold value. Then, image tone such as soft, hard, standard, etc. is selected. An adequate voltage within the range of the application voltage is set as the standard application voltage, and image recording is performed. In this case, the time of voltage application can be controlled by monitoring transmittance or current value of the liquid crystal to find out that the voltage on the exposed portion has reached the threshold voltage. The image thus recorded is read, and the application voltage is adjusted until the image tone agrees with the desired tone. Then, the image recording is completed.

As described above, it is possible according to the present invention to control recording characteristics of an image to be recorded by changing voltage applying conditions and to record the image by setting the optimal application voltage.

What I claim is:

1. A photographing method, comprising a photo sensor having a photoconductive layer formed on a transparent electrode and a liquid crystal recording medium having a liquid crystal polymer composite layer consisting of a resin and a liquid crystal formed on an electrode, said photo sensor and said liquid crystal recording medium placed face-to-face with an air gap therebetween to form a separate type information recording medium, image exposure is performed to the photo sensor, said liquid crystal is oriented by applying voltage between the two electrodes, and image information is recorded, whereby;

an application voltage, at which initial distribution voltage to the liquid crystal medium determined by capacities of the liquid crystal medium and the photo sensor is ½ or less of threshold voltage of the liquid crystal medium, is defined as an upper limit application voltage;

a sum V1 of saturation voltage of the liquid crystal medium and breakdown voltage, or an application voltage V2 where equilibrium potential of the liquid crystal medium obtained from resistance of the photo sensor based on base current of the photo sensor and from resistance of the liquid crystal medium is higher than the threshold voltage, whichever is higher, is defined as a lower limit application voltage; and

an image is recorded by setting the application voltage between the upper limit application voltage and the lower limit application voltage.

2. A photographing method according to claim 1, wherein image characteristics are controlled by changing the application voltage within said preset range.

3. A photographing apparatus, comprising a photo sensor having a photoconductive layer formed on a transparent electrode and a liquid crystal recording medium having a liquid crystal polymer composite layer consisting of resin and liquid crystal formed on an electrode, said photo sensor and said liquid crystal recording medium placed face-to-face with an air gap therebetween to form a separate type information recording medium, image exposure is performed to the photo sensor, said liquid crystal is oriented by applying voltage between the two electrodes, and image information is recorded, whereby there are provided:

means for measuring resistance of the liquid crystal medium, means for determining base current of the photo sensor, and control means for setting application voltage range;

said control means calculates an upper limit application voltage, defined as a voltage, at which initial distribution voltage to the liquid crystal medium determined by capacities of the liquid crystal medium and the photo sensor is ½ or less of the threshold voltage of the liquid crystal medium, and also calculates a lower limit application voltage defined as a sum V1 of saturation voltage of the liquid crystal medium and breakdown voltage, or an application voltage V2 where equilibrium potential of the liquid crystal medium obtained from resistance of the photo sensor based on base current of the photo sensor and from resistance of the liquid crystal medium is higher than the threshold voltage, whichever is higher, and the application voltage is controlled within the range of said upper limit application voltage and said lower limit application voltage.

* * * * *

APPENDIX H

***Oh* Reference**

U.S. Patent No. 6,466,204

US006466204B1

(12) **United States Patent**
Oh

(10) **Patent No.: US 6,466,204 B1**
(45) **Date of Patent: Oct. 15, 2002**

(54) **COLOR LCD INTERFACE CIRCUIT IN A PORTABLE RADIO TERMINAL**

(75) Inventor: **Jeong-Seok Oh**, Yongin-shi (KR)

(73) Assignee: **Samsung Electronics, Co., Ltd.** (KR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/482,506**

(22) Filed: **Jan. 13, 2000**

(30) **Foreign Application Priority Data**

Jan. 13, 1999 (KR) 99-663

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(52) **U.S. Cl.** **345/213**; 455/556; 379/88.17
(58) **Field of Search** 345/213, 88, 204; 455/566, 426, 556, 557; 379/88.13, 88.17, 900

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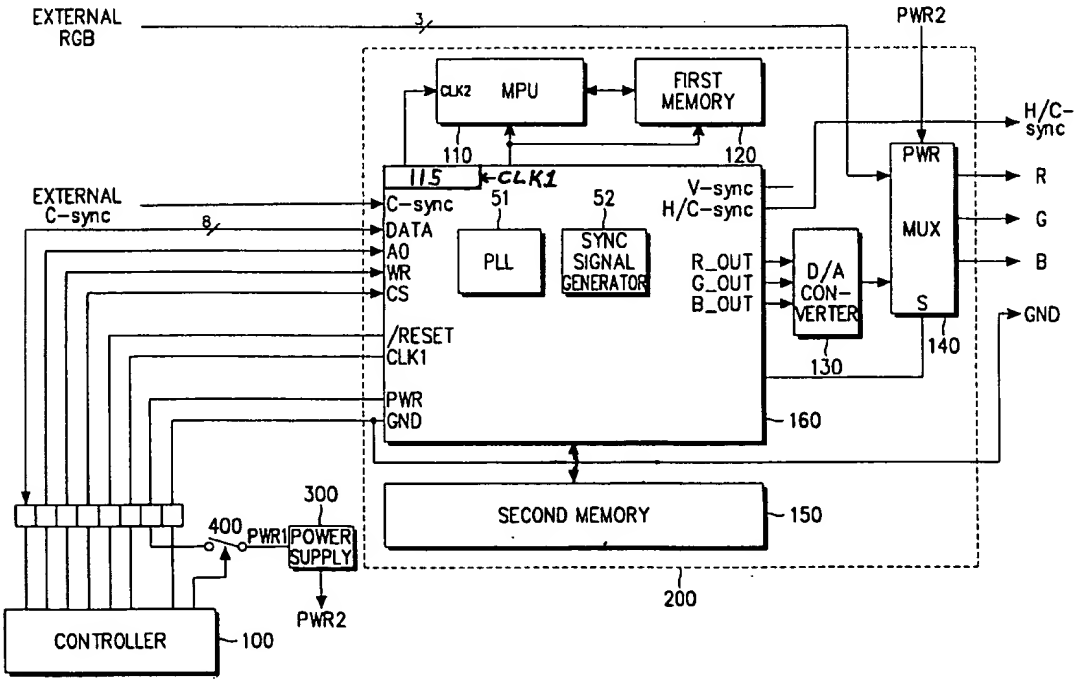
(57) **ABSTRACT**

There is provided a color LCD (Liquid Crystal Display) interface circuit for outputting an RGB (Red, Green, Blue) signal for an intended image and a synchronization signal for either a horizontal and vertical synchronization or a composite synchronization to a color LCD controller in a portable radio terminal which has a color LCD and a controller and supports a character-type black and white LCD. In the color LCD interface circuit, a first memory stores data needed to execute a color LCD interface program and to represent fonts and color, a main controller reads the color LCD interface program from the first memory and executes the color LCD interface program, a second memory stores a page of image information generated during executing the color LCD interface program, a multiplexer selects one of input signals according to whether a graphical display on the color LCD is a picture or represents the operational status of the portable radio terminal, and a color processor receives various commands and index data from the controller and generates an internal composite synchronization signal and a digital RGB signal.

4 Claims, 1 Drawing Sheet



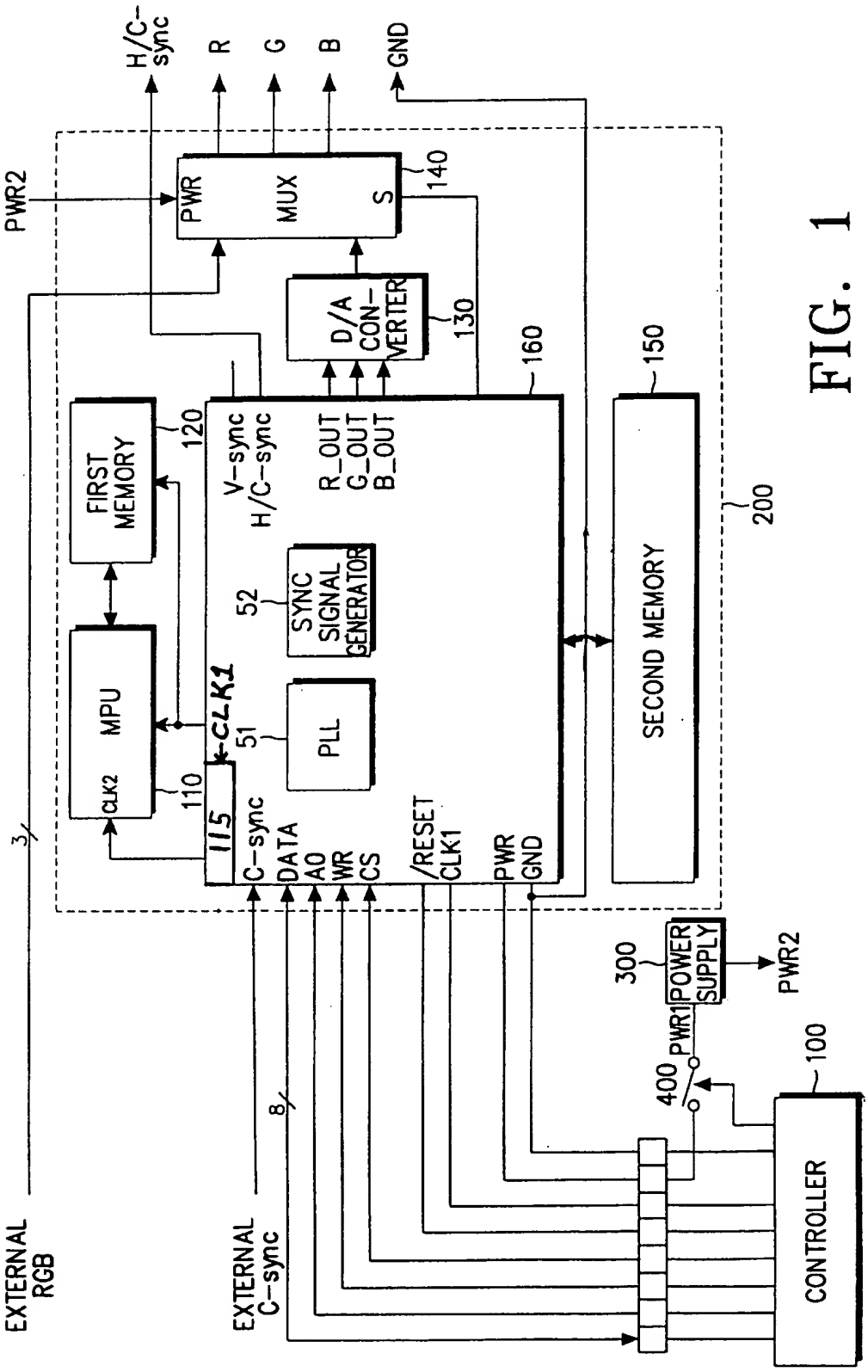

H/C-sync
R
G
B
GND
PWR2
PWR
MUX
S
140
D/A CON-VERTER
130
160
150
FIRST MEMORY
120
V-sync
H/C-sync
R_OUT
G_OUT
B_OUT
200
SECOND MEMORY
SYNC SIGNAL GENERATOR
52
MPU
CLK2
CLK1
PLL
51
110
115
C-sync
DATA
A0
WR
CS
/RESET
CLK1
PWR
GND
3
8
300
POWER SUPPLY
PWR2
PWR1
400
100
CONTROLLER
EXTERNAL RGB
EXTERNAL C-sync

FIG. 1

COLOR LCD INTERFACE CIRCUIT IN A PORTABLE RADIO TERMINAL

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to a display in a portable radio terminal, and in particular, to an interface circuit of a color LCD (Liquid Crystal Display) for displaying pictures or characters.

2. Description of the Related Art

As the performance of communication terminals (mobile phones) improves, they are capable of transmitting not only voice communication but also data and image communication as well. To provide the image communication service, the standard character-type black and white LCD is replaced with a color LCD. Because of the large power dissipation of an OSD (On Screen Display), the typical television OSD is difficult to apply to a communication terminal (mobile phone) which requires minimum power consumption. A low power consumption alternative, like the LCD, is needed. Unfortunately, the conventional control devices cannot be applied to the color LCD, therefore, a new color LCD interface is needed. While constructing an RGB (Red, Green, Blue) signal and a synchronization circuit represents a significant undertaking, the present invention addresses this problem.

SUMMARY OF THE INVENTION

It is, therefore, an object of the present invention to provide an interface circuit in a portable radio terminal (mobile phone) for interfacing between a color LCD controller and a portable radio terminal controller. The output circuit consists of a signal suitable for a conventional LCD controller or a color LCD. A conventional character-type LCD may therefore be replaced with a color LCD without incident.

To achieve the above, there is provided a color LCD interface circuit for outputting an RGB signal for an intended image and either a synchronization signal for horizontal and vertical synchronization or a composite synchronization signal to a color LCD controller in a portable radio terminal. The interface circuit is compatible with portable radio terminals having either a color LCD and a controller or a character-type black and white LCD. In the color LCD interface circuit, a first memory stores data needed to execute a color LCD interface program and to represent fonts and color. A main controller reads the color LCD interface program from the first memory and executes the color LCD interface program while a second memory stores a page of image information generated during the execution of the color LCD interface program. A multiplexer selects one of the input signals according to whether a graphical display on the color LCD is an image or represents the operational status of the portable radio terminal. A color processor receives various commands and index data from the controller and generates an internal composite synchronization signal and a digital RGB signal.

BRIEF DESCRIPTION OF THE DRAWING

The above and other objects, features and advantages of the present invention will become more apparent from the following detailed description when taken in conjunction with the accompanying drawing in which:

FIG. 1 is a block diagram of a color LCD interface circuit in a portable radio terminal according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A preferred embodiment of the present invention will be described hereinbelow with reference to the accompanying drawings. In the following description, well-known functions or constructions are not described in detail since they would obscure the invention in unnecessary detail.

Referring to FIG. **1**, reference numeral **100** denotes a portable radio terminal controller (hereinafter, referred to as a controller), which can be an MSM (Mobile Station MODEM). An LCD interface circuit **200** includes: a microprocessor unit (MPU) **110**, a first memory **120**, a digital-to-analog (D/A) converter **130**, a multiplexer **140**, a second memory **150**, and a color processor **160**. Reference numeral **300** denotes a power supply for supplying power to the LCD interface circuit **200**. A switch **400**, operating under the control of controller **100**, connects the color LCD interface circuit operating voltage (e.g., 3.3.V) from a power supply terminal PWR1 to circuit **200**. The multiplexer **140** should operate all the time and therefore receives a DC (Direct Current) voltage (e.g., 3.3V) from the power supply **300** through a power supply terminal PWR2. PWR1 and PWR2 are identical though they are separately described for the sake of convenience.

The color LCD interface circuit **200** generates an RGB signal for an intended image and either a synchronization signal for horizontal synchronization and vertical synchronization, or a composite synchronization signal, and feeds these signals to an LCD controller (not shown).

The first memory **120** can be a ROM and is used to store a color LCD interface program and initial data. The initial data refers to fonts or other data needed for representing **256** colors. It is understood that one skilled in the art may modify the present invention to display more or less colors without departing from the spirit and scope of the present invention. The MPU **110** reads the color LCD interface program from the first memory **120** and executes the program.

The second memory **150** can be a RAM and temporarily stores any data required to implement the color LCD interface program, for example, information about a page of images.

The D/A converter **130** converts the digital RGB output of the color processor **160** to analog data. It is determined whether to output a signal in an analog or digital form depending on the form of an LCD input. In the embodiment of the present invention, the D/A converter **130** is used to output a signal in an analog form. If the LCD requires digital inputs, the D/A converter **130** is not necessary.

The multiplexer **140** selects one of the input signals according to whether a graphical display on the color LCD is an image like a photograph or represents the operational status of the portable radio terminal. That is, the multiplexer **140** selects between the RGB signal from the D/A converter **130** and an external RGB signal.

The color processor **160** outputs a composite synchronization signal C-sync and a digital RGB signal, for the input of 8-bit data DATA, a chip select signal CS, a write signal WR, a busy check signal AO, and a reset signal /RESET which are provided to a conventional character-type black and white LCD controller by the controller **100**. The color LCD interface circuit **200** can output a composite synchronization signal C-sync alone or both vertical and horizontal synchronization signals according to the specification of a color LCD. 'H/C-sync' in the drawing indicates that a port can be designed to be shared for outputting a horizontal synchronization signal or a composite synchronization signal C-sync.

A clock divider **115** divides a first clock signal CLK1 received from the controller **100** by a predetermined value, and feeds the divided signal to the MPU **110** as an operational clock (hereinafter, referred to as a second clock signal CLK2). For example, a first clock signal CLK1 of 27 Mhz can be divided by 2, thereby producing a second clock signal CLK2 of 13.5 Mhz.

The color processor **160** includes a phase locked loop (PLL) **51** and a synchronization signal generator **52**. The synchronization signal generator **52** generates a vertical synchronization signal and a composite synchronization signal (an internal composite synchronization signal to be distinguished from an external composite synchronization signal for displaying a background). In addition, the C-sync signal refers to a signal containing H-sync and V-sync. A horizontal synchronization signal can be produced by use of the two synchronization signals. The PLL **51** controls the phase of the internal composite synchronization signal to compensate for the phase difference between the internal and external composite synchronization signals.

The operation of the color LCD interface circuit in the portable radio terminal according to the embodiment of the present invention will now be described in detail.

Two cases can be considered: first, displaying only characters in color, and second, displaying characters and a background in color. The former case needs only an external composite synchronization signal, obviating the need for operating the PLL **51**.

The following description is confined to the latter case. An external RGB signal and a composite synchronization signal C-sync are input for displaying a background. The controller **100** outputs a predetermined command and index data to the color LCD interface circuit **200** in order to display the intended characters on a color LCD. The MPU **110** of the color LCD interface circuit **200** interprets the command and the index data, reads a corresponding font from the first memory **120**, and writes the font in an intended position of the second memory **150**. That is, a character desired by a user is written.

Commands received at the color LCD interface circuit **200** from the controller **100** are processed by the MPU **110**. The processing of the MPU **110** includes: interpreting a corresponding command and determining which operation to execute, reading the font, character color, and background color from the first memory **120** according to the determination, and constructing a page of images in the second memory **150**. The images are then displayed.

In accordance with the present invention as described, a portable radio terminal controller can output a signal suitable for either a conventional character-type black and white LCD display or a color LCD, without any modification, simply by using the interface circuit of the present invention.

While the invention has been shown and described with reference to a certain preferred embodiment thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

What is claimed is:

1. A color LCD (Liquid Crystal Display) interface circuit for outputting an RGB (Red, Green, Blue) signal for an intended image and either a synchronization signal for horizontal and vertical synchronization or a composite synchronization signal to a color LCD controller in a portable radio terminal having a color LCD and a terminal controller, the circuit comprising:

a first memory for storing data needed to execute a color LCD interface program and to represent fonts and color;

a main controller for reading the color LCD interface program from said first memory and executing said color LCD interface program;

a second memory for storing a page of image information generated during the execution of said color LCD interface program;

a color processor for receiving various commands and index data from the terminal controller and generating an internal composite synchronization signal and a digital RGB signal; and

a multiplexer for selecting one of the input signals according to whether a graphical display on the color LCD is a picture or represents the operational status of the portable radio terminal, said first input signal being an external RGB signal, and said second input signal being said digital RGB signal generated by said color processor.

2. The color LCD interface circuit of claim **1**, further comprising a digital-to-analog converter for converting the digital RGB signal received from the color processor to an analog signal.

3. The color LCD interface circuit of claim **1**, wherein the color processor receives a first clock signal from the terminal controller and a clock divider located within the color processor divides the first clock signal by a predetermined value, and outputs the divided signal to the main controller.

4. The color LCD interface circuit of claim **1**, wherein the color processor comprises:

a synchronization signal generator for generating the internal composite synchronization signal; and

a phase locked loop for controlling the phase of the internal composite synchronization signal to compensate for a phase difference between an external composite synchronization signal and the internal composite synchronization signal.

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